MODEL NAME : *BCV00/ BCV10*

PCB NO : *LA-D991P*

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

For Dell Review only

2016-06-25

Rev: 1.0 (A00)

@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
EMC@ : Pop of EMI parts
M2G@ : Micron GDDR5 2G for GPU
H2G@ : Hynix GDDR5 2G for GPU
S4G@ : Samsung GDDR5 4G for GPU
M4G@ : Micron GDDR5 4G for GPU
BreakDown@ : For measure power consumption
14GT@ : 14" GPU N16P-GT
15GX@ : 15" GPU N16P-GX

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Issued Date	2011/08/25	Deciphered Date	2011/08/25	Title: Cover Page
				Size: Document Number: Rev: 0.1(A00)
				Date: Thursday, August 18, 2016 Sheet 1 of 70

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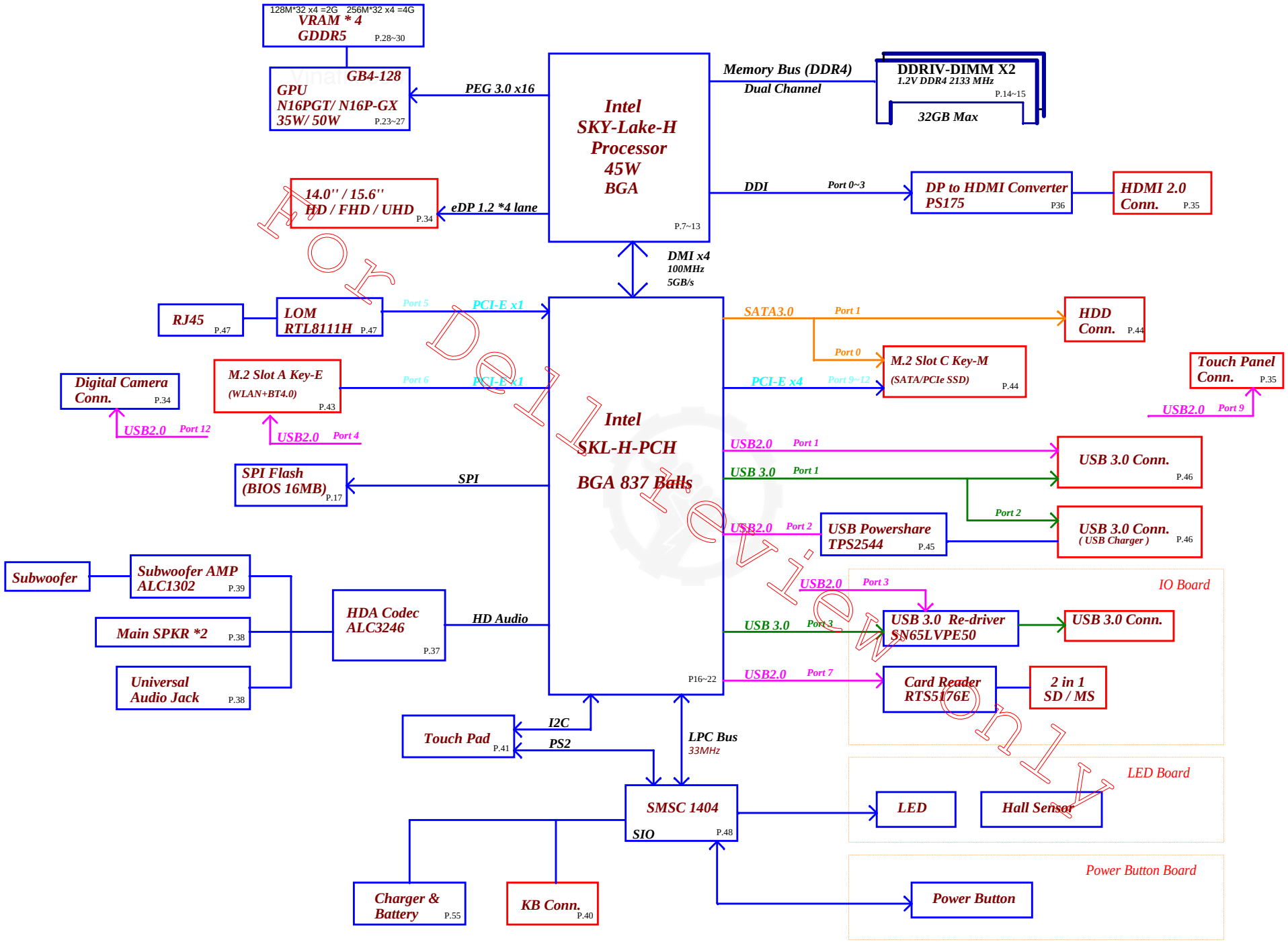

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Compal Electronics, Inc.

Title: **Block diagram**

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 2 of 70

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Project Code :
File Name :

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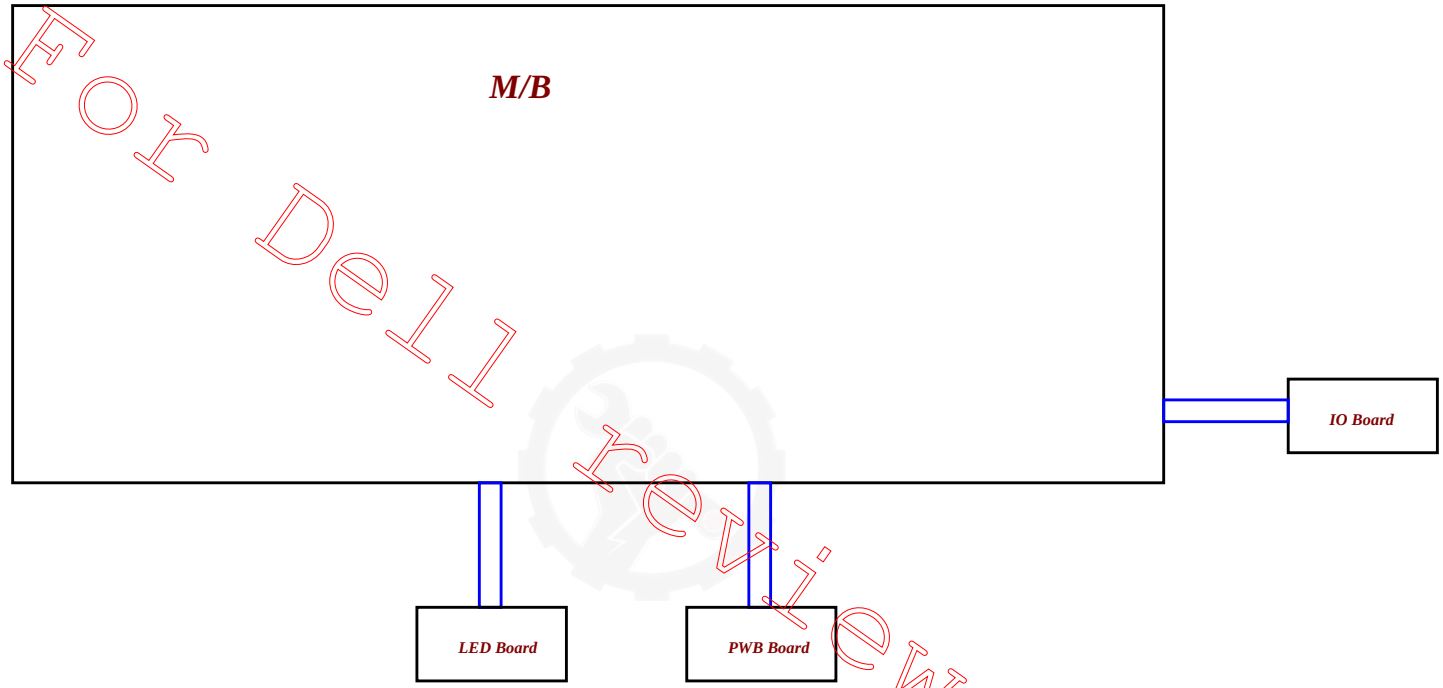

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Compal Electronics, Inc.

Title: **DB block diagram**

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 3 of 70

Board ID	Resistor
X00	10K
X01	13.7K
X02	17.8K
X03	
A00	22.1K

USB3	DESTINATION
1	USB Conn 1
2	USB Conn 2
3	USB Conn 3 (IO Board)
4	None
5	None
6	None
7	None
8	None
9	None
10	None

USB 2.0	DESTINATION
1	USB Conn 1
2	USB Conn 2
3	USB Conn 3 (IO Board)
4	NGFF1- WLAN
5	None
6	None
7	Card Reader
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Converter
2	Converter
3	Converter

LPC	DESTINATION
LPC0	MEC1404
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	LAN
Lane 6	WLAN
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	None
Lane 16	None

SATA	DESTINATION
0A	SSD
1A	SSD
N/A	N/A
N/A	N/A
0B	None
1B	HDD
2	None
3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	LAN	12	GPU
3	NGFF-1 WLAN	13	None
4	None	14	None
5	None	15	None
6	NGFF-2 SSD		
7	None		
8	None		
9	None		

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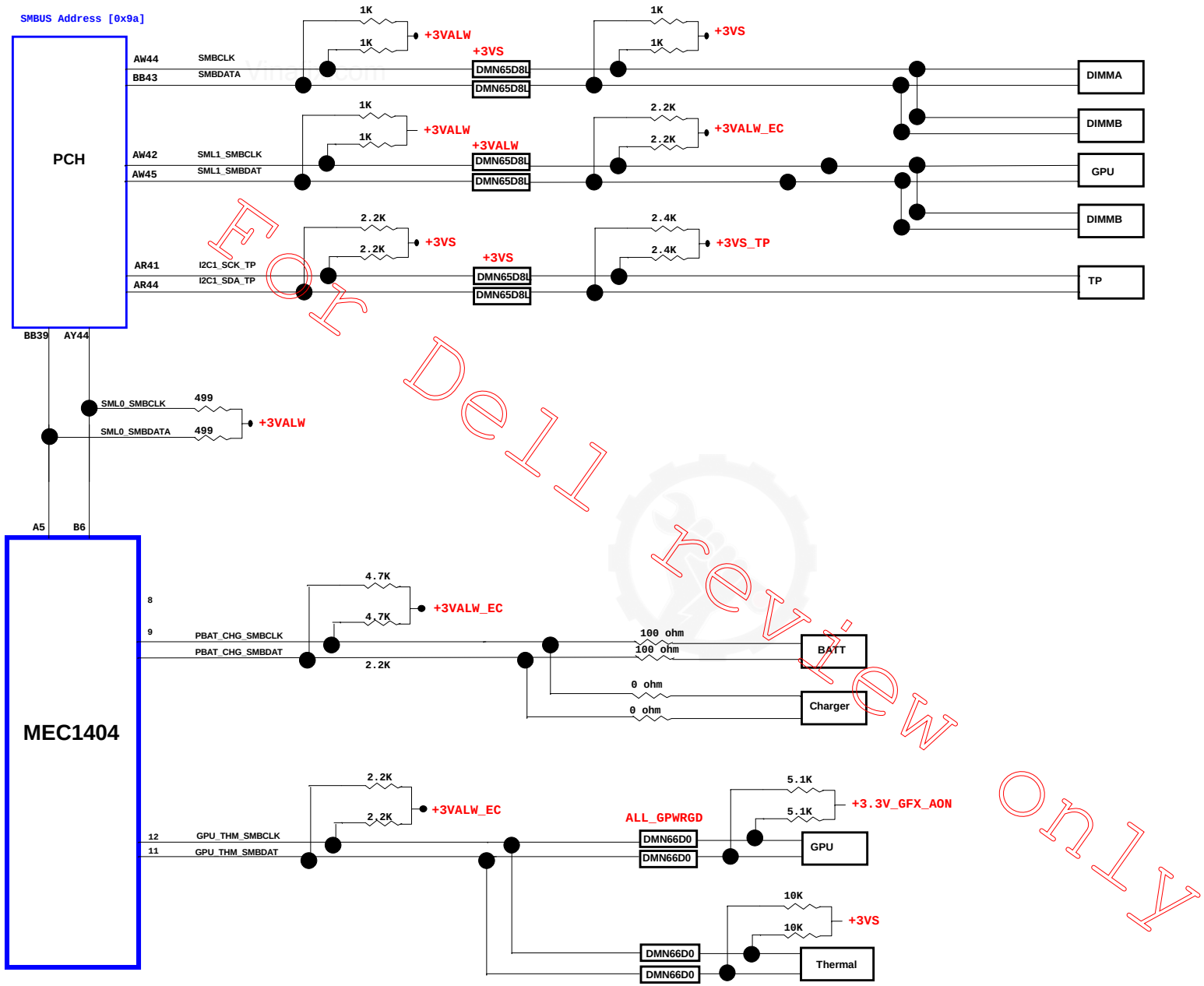
Symbol Note :

: means Digital Ground

: means Analog Ground



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Title: **SMBus Block Diagram**

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Date: Thursday, August 18, 2016 | Sheet 5 of 70

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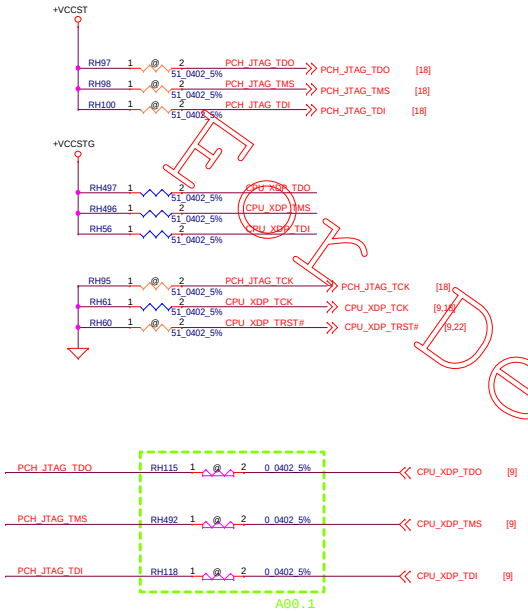

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		0.1(X00)

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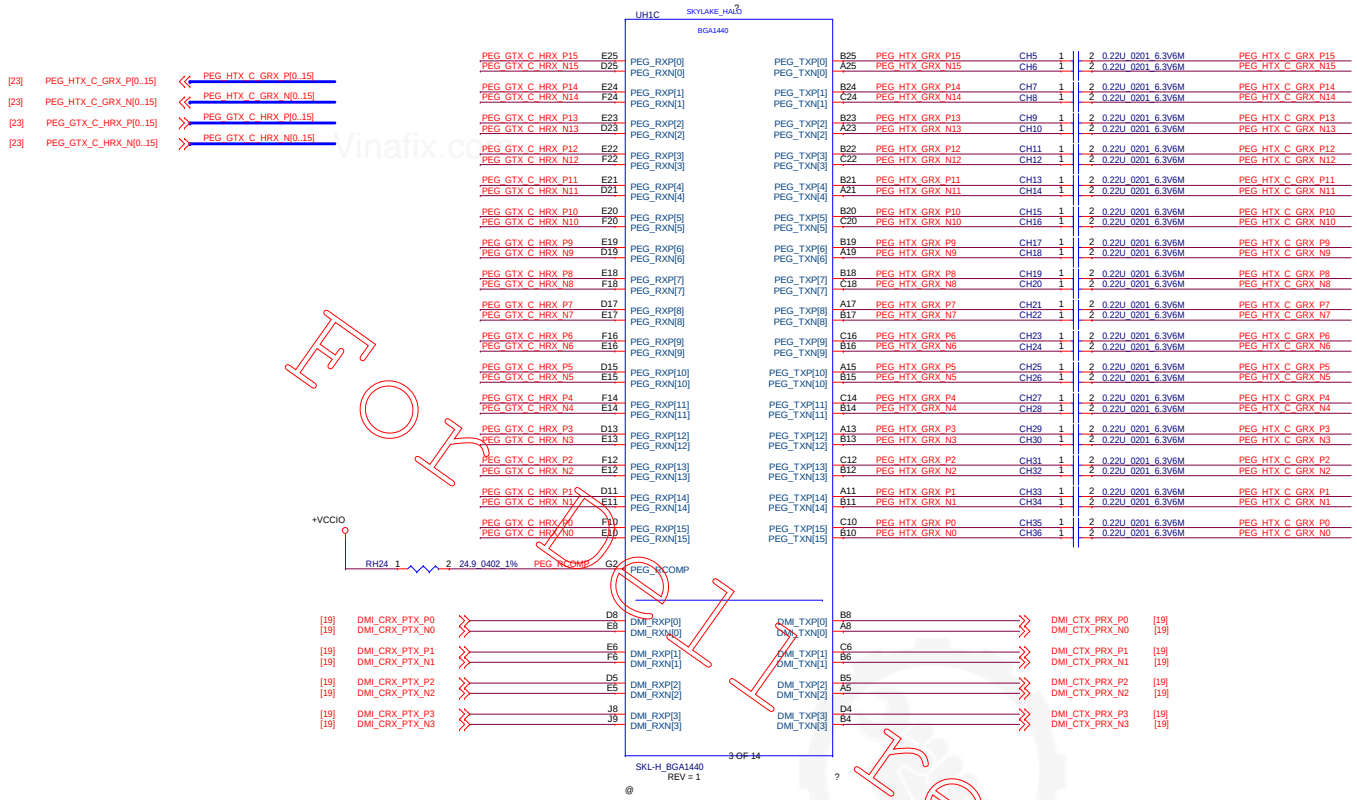

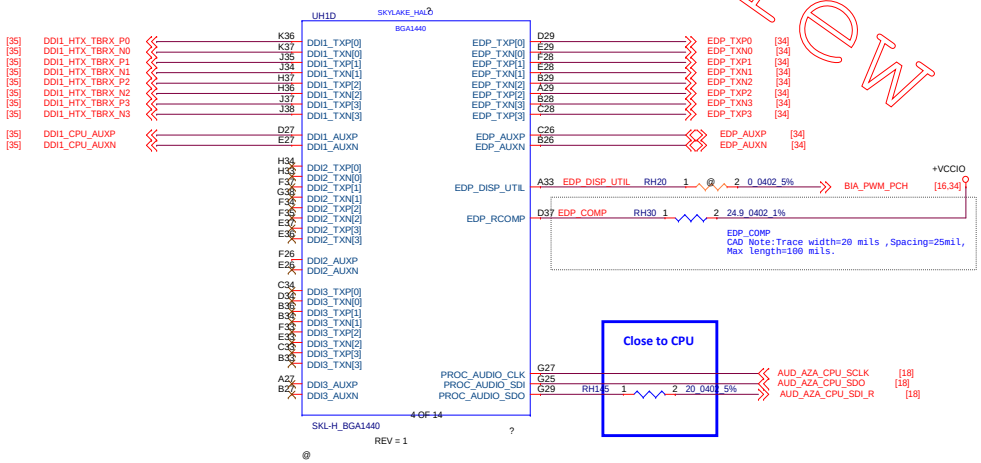

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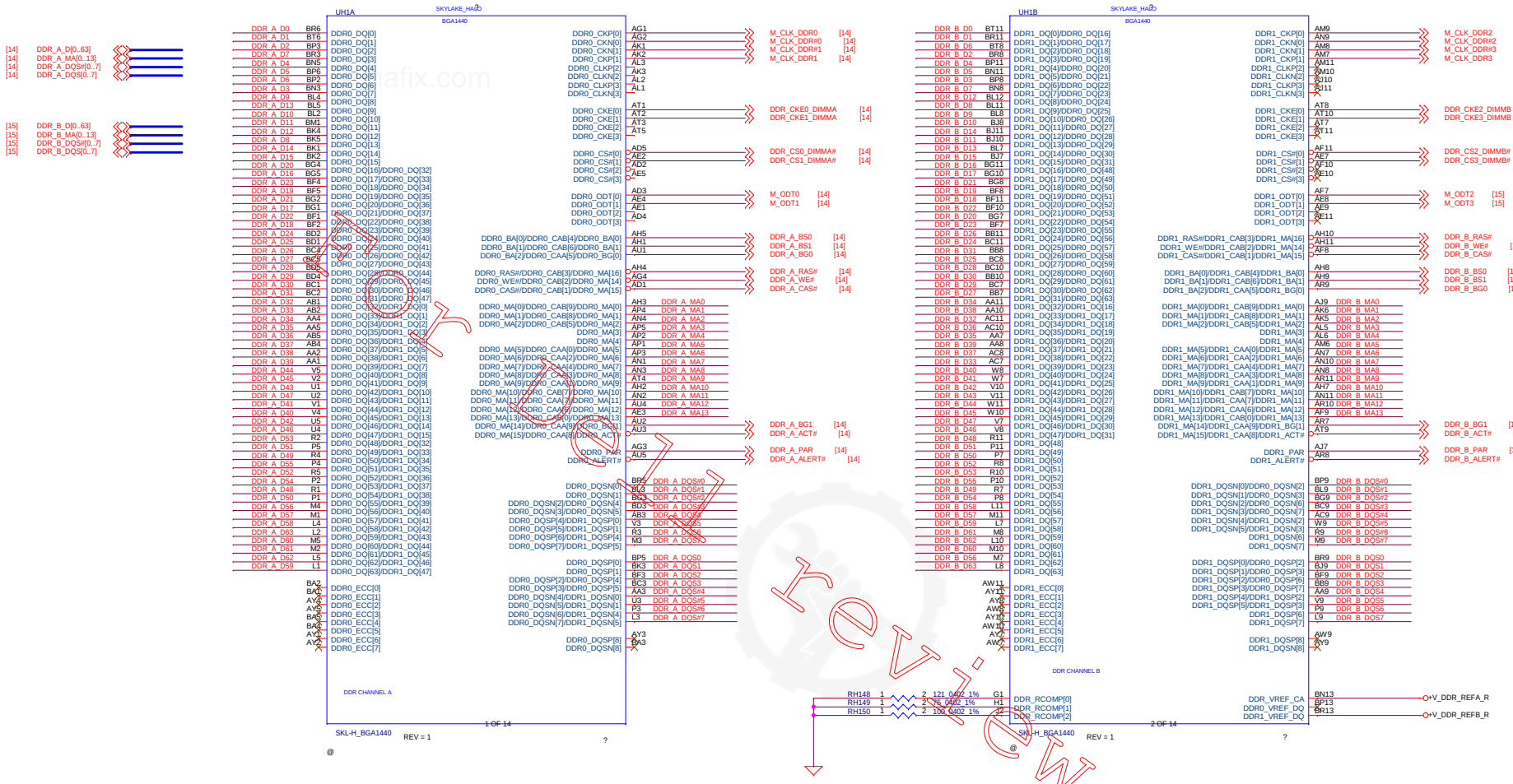
Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: C | Document Number | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 7 of 70

Interleave



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Title: **PROCESSOR(3/7) DDRIII**

Size: C | Document Number | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 8 of 70

CFG Straps for Processor

Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

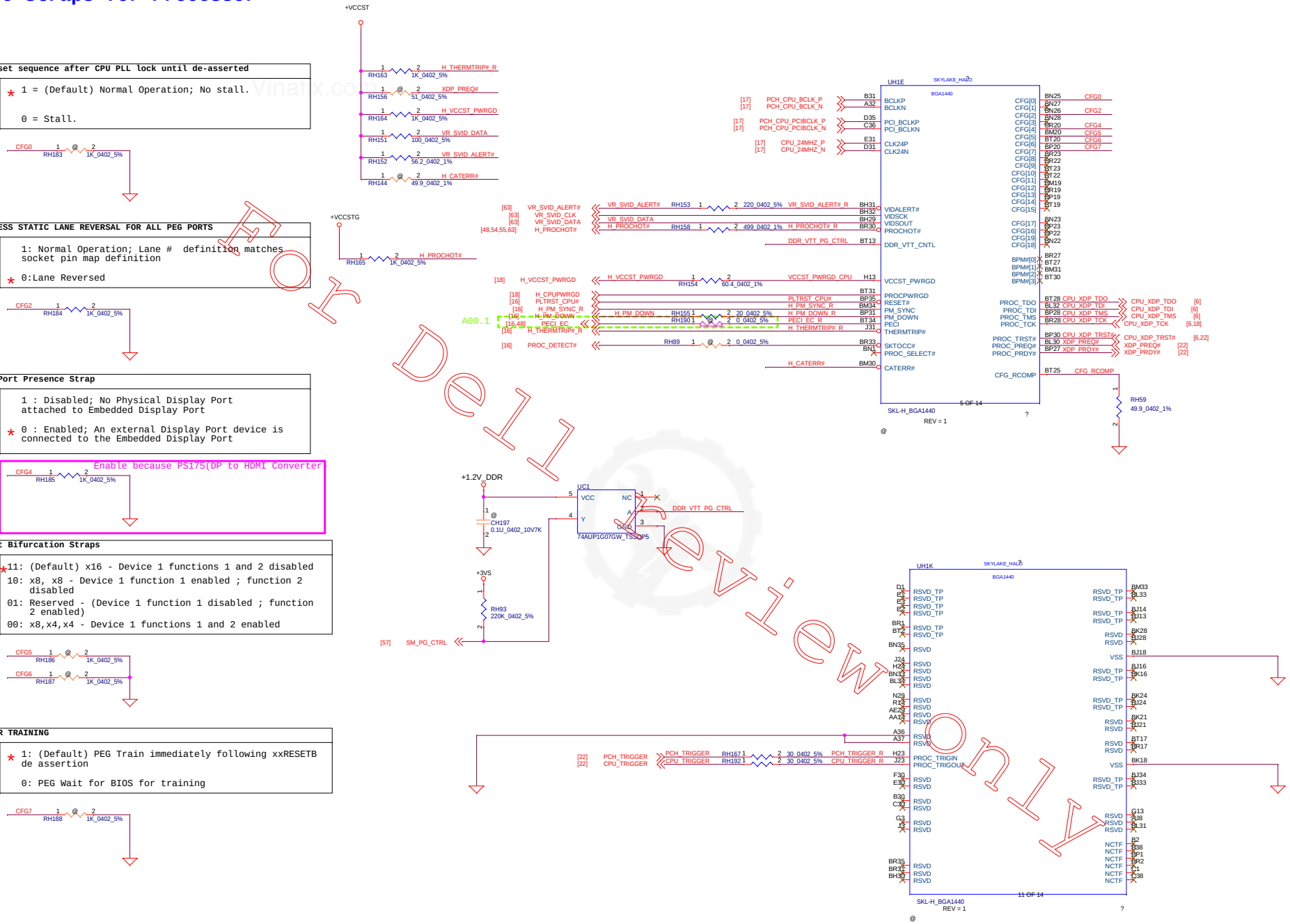
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Enable because PS175(DP to HDMI Converter

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: C | Document Number | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 9 of 70

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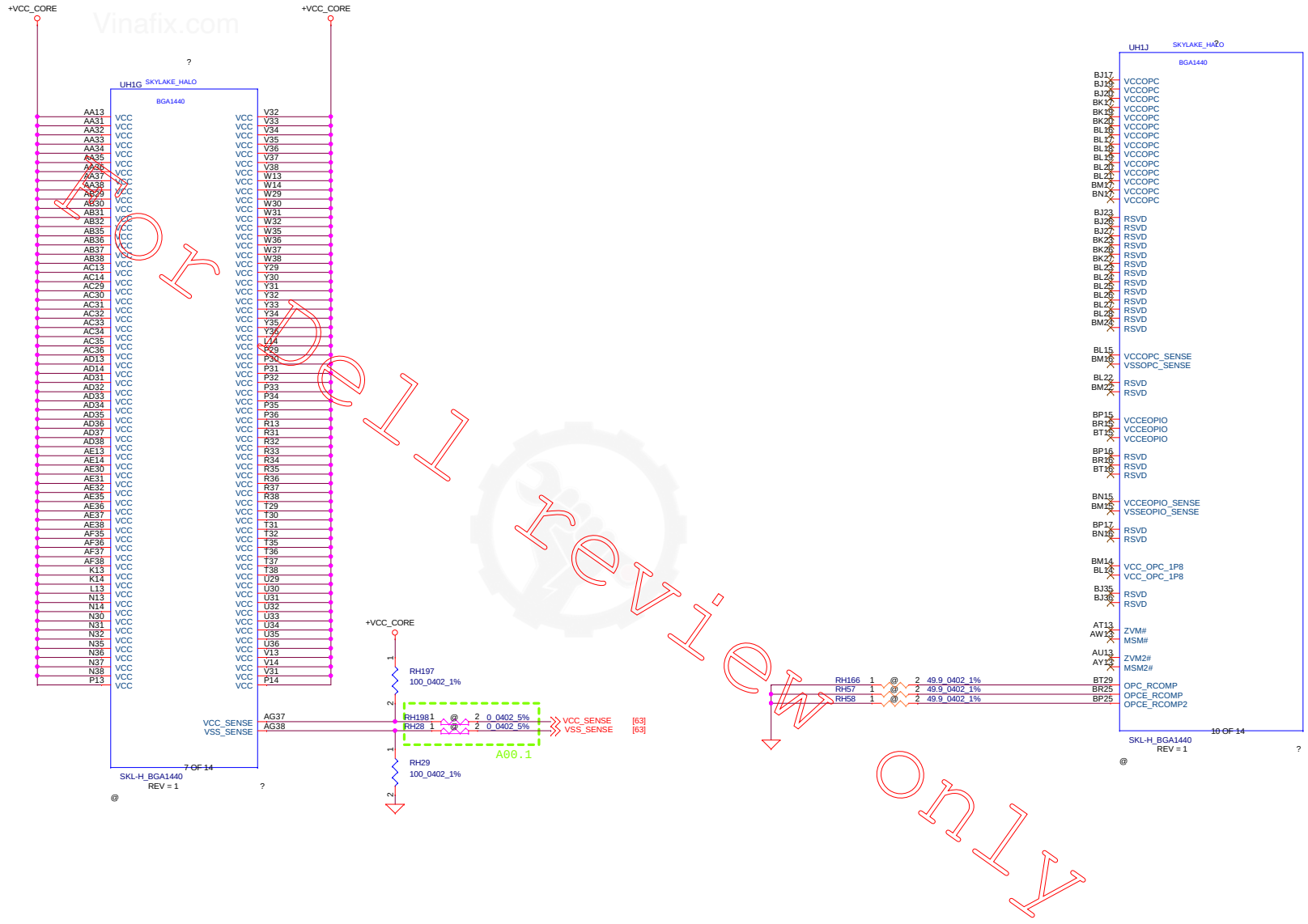

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Title: **PROCESSOR(5/7) PWR,BYPASS**

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Custom		0.1(X00)

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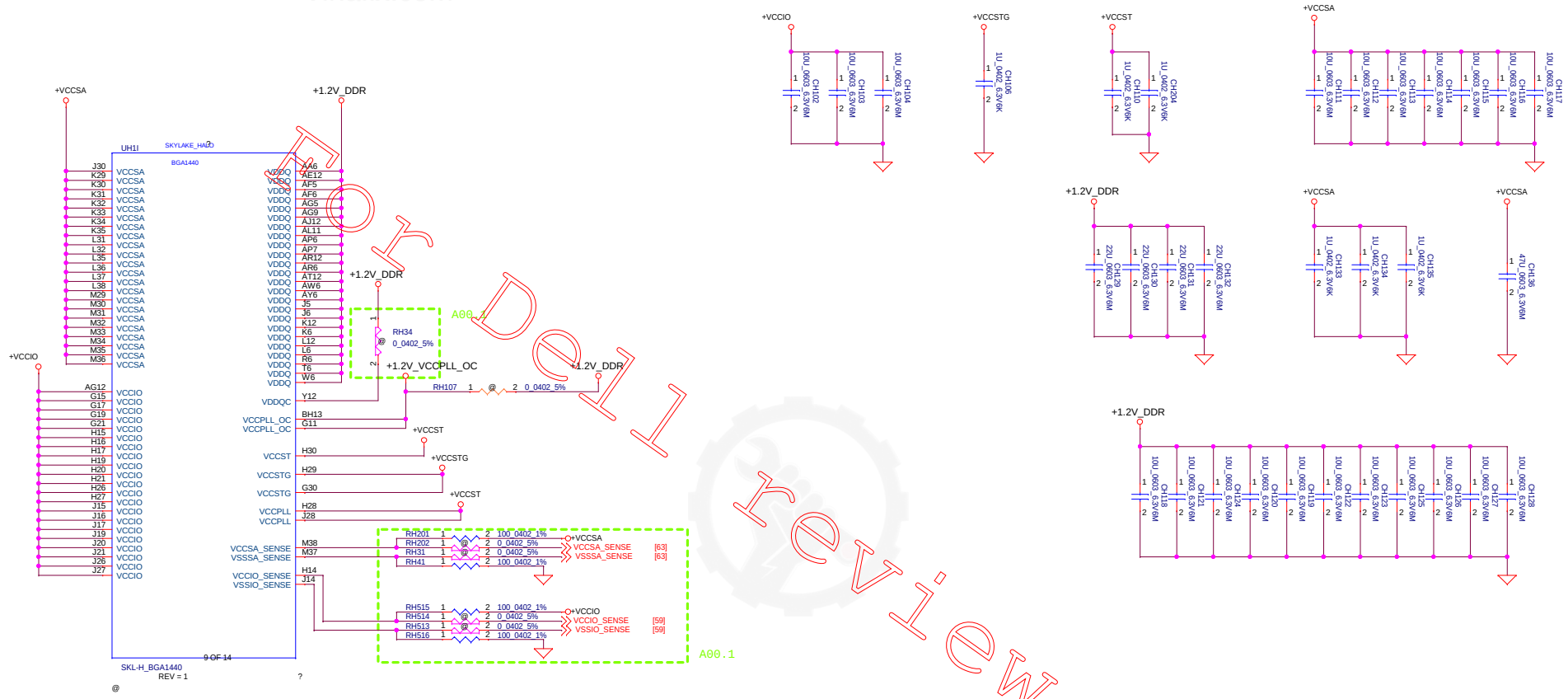

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Title: **PROCESSOR(6/7) PWR**

Size: Custom | Document Number | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 11 of 70

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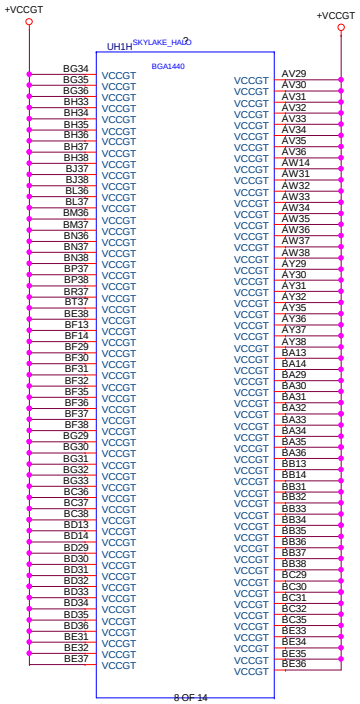

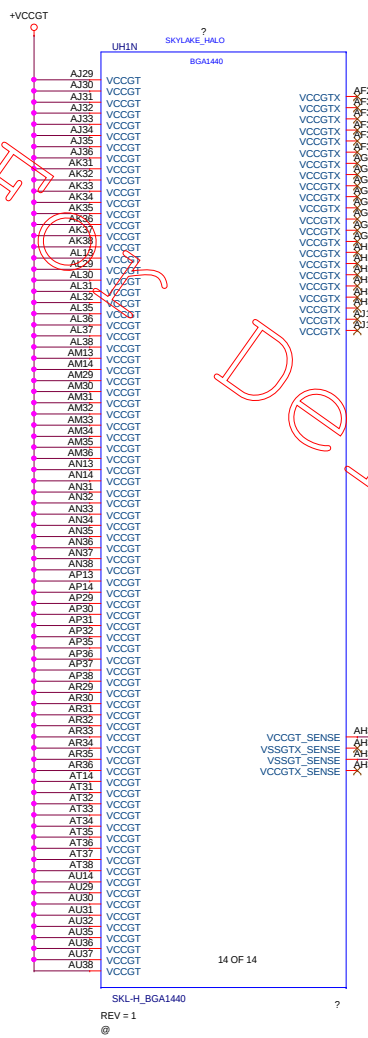

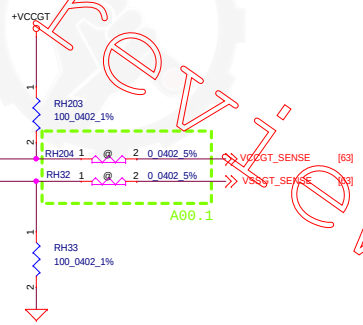

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Title: **PROCESSOR(2/7) PM,XDP,CLK**

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Title: **PROCESSOR(7/7) VSS**

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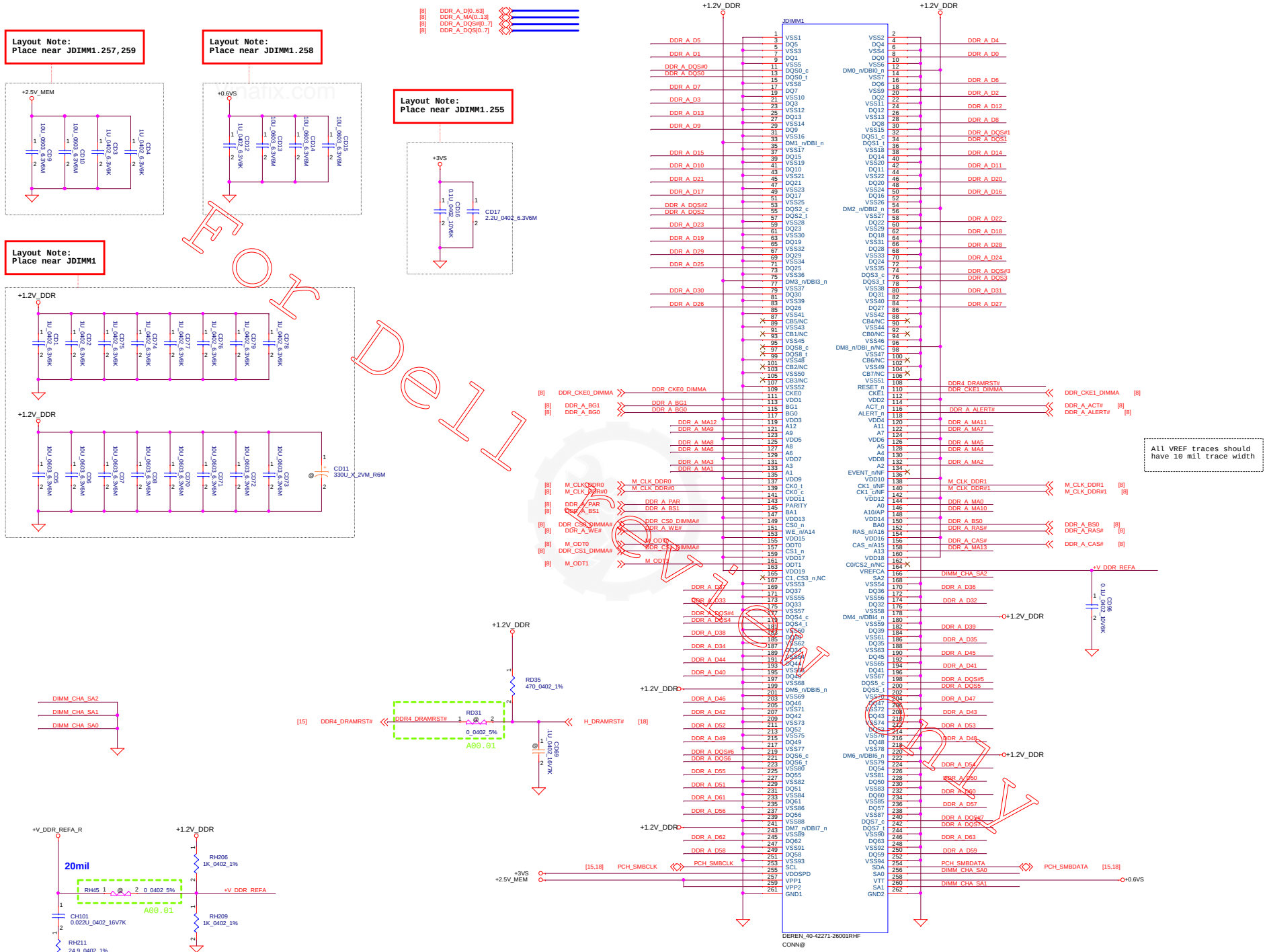

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Title: **DDRIII DIMMA**

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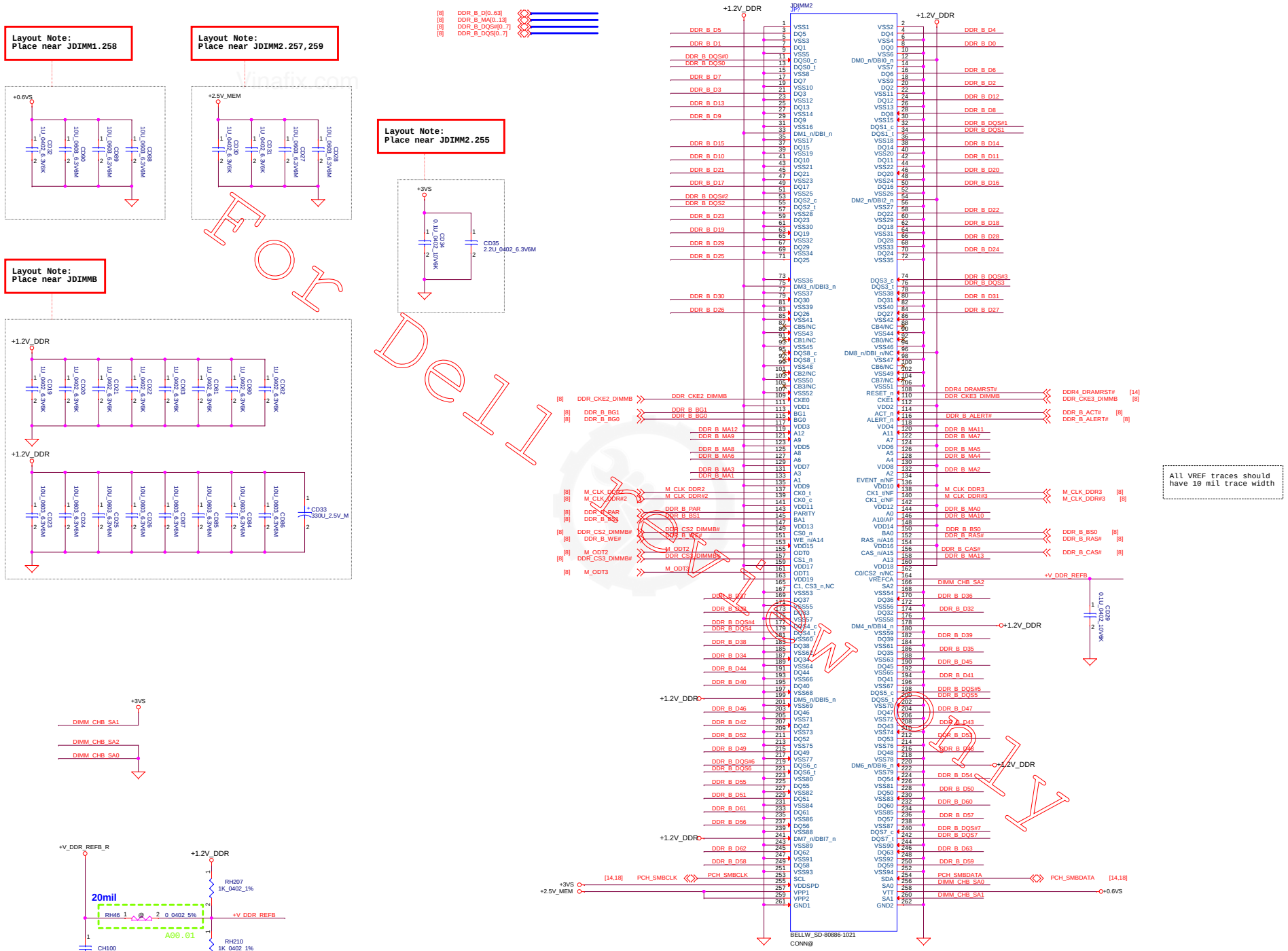

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Title: DDRIII DIMMB

Size: | Document Number: LA-D991P | Rev: 0.1(DD)

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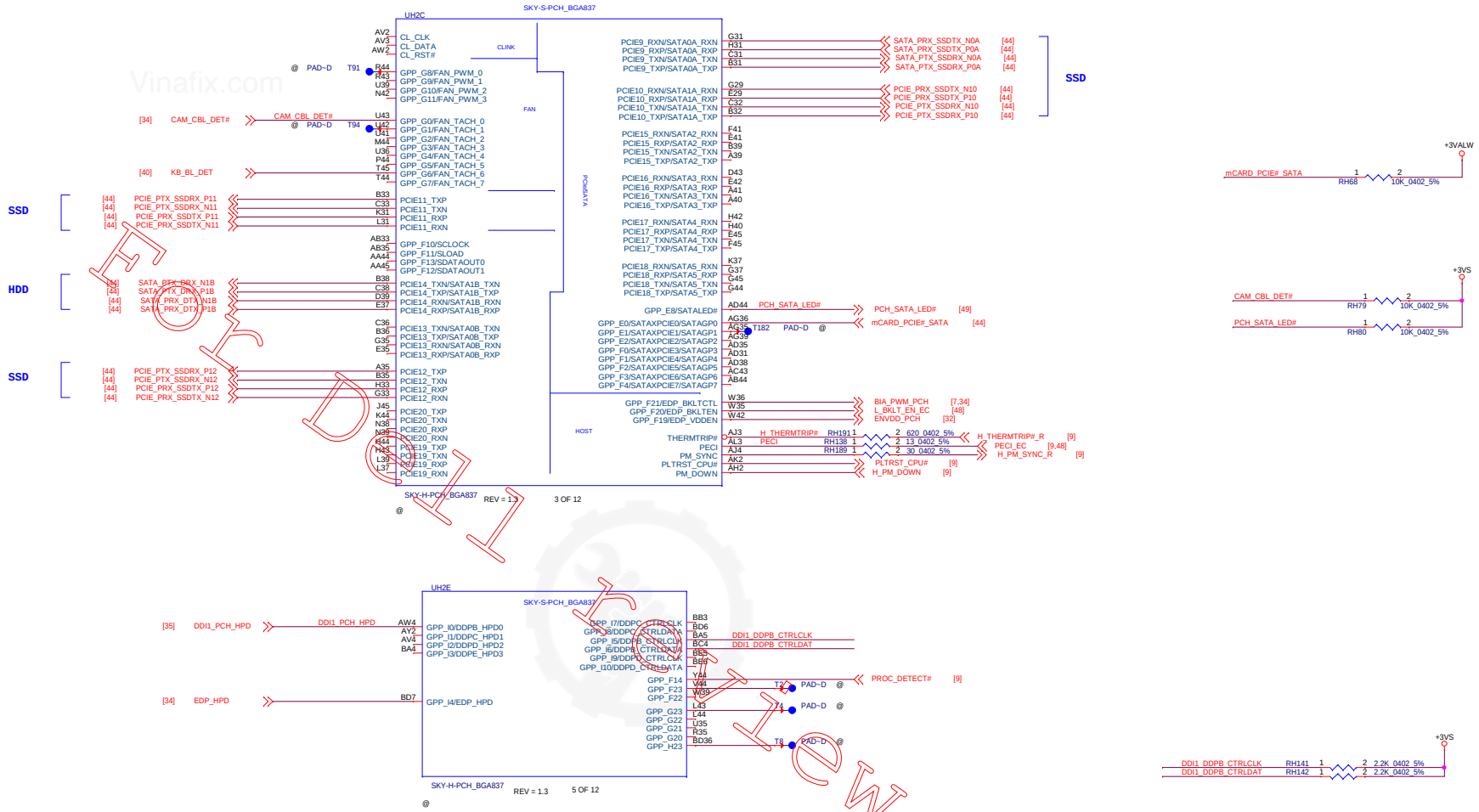

PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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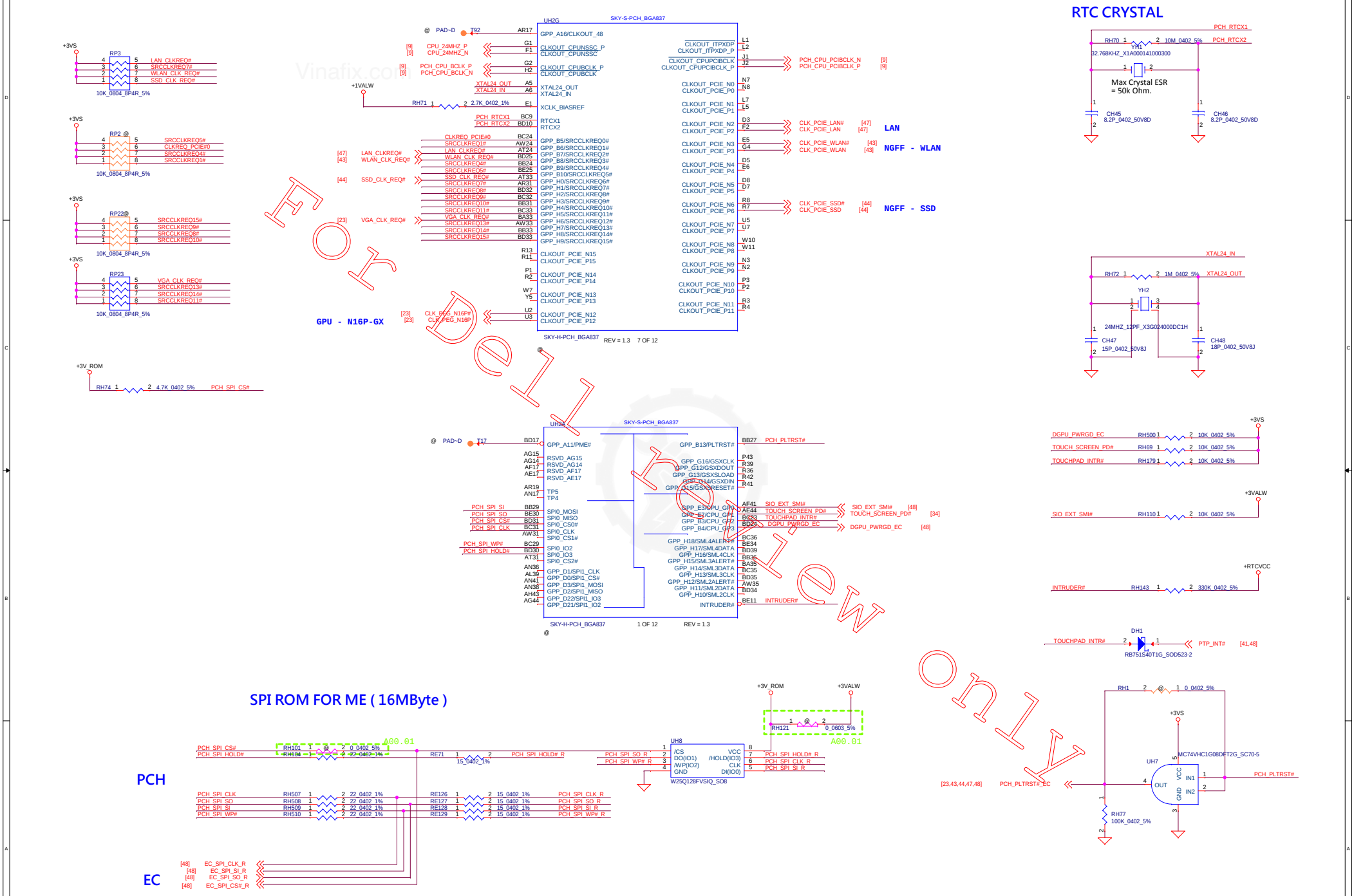
Title: **PCH (1/8) SATA,HDA**

Size: | Document Number: **LA-C361P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 16 of 70



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Title: **PCH (2/8) SMBUS, CLK, SPI, LPC**

Size: | Document Number: **LA-D991P** | Rev: 0.1(X00)

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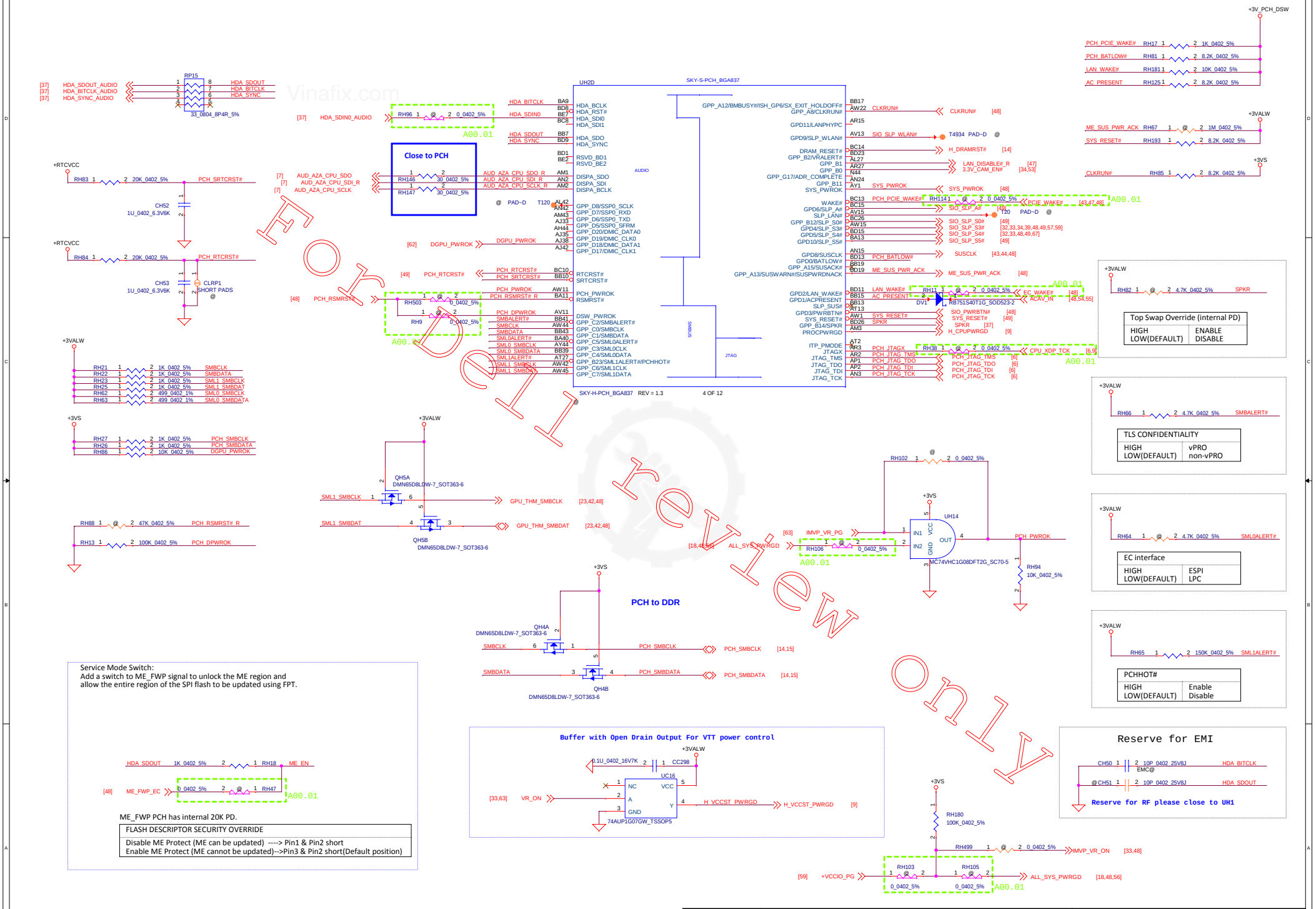

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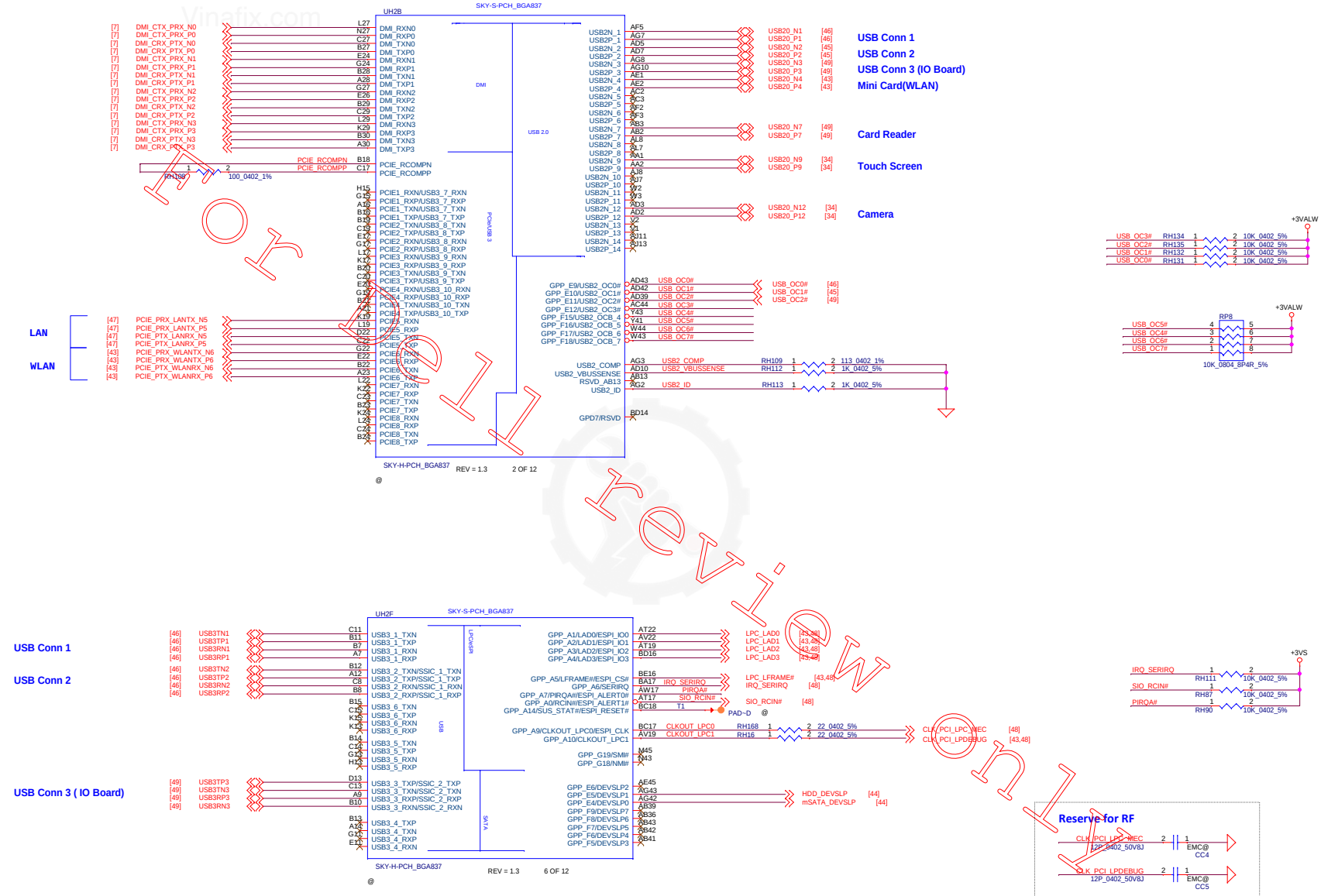

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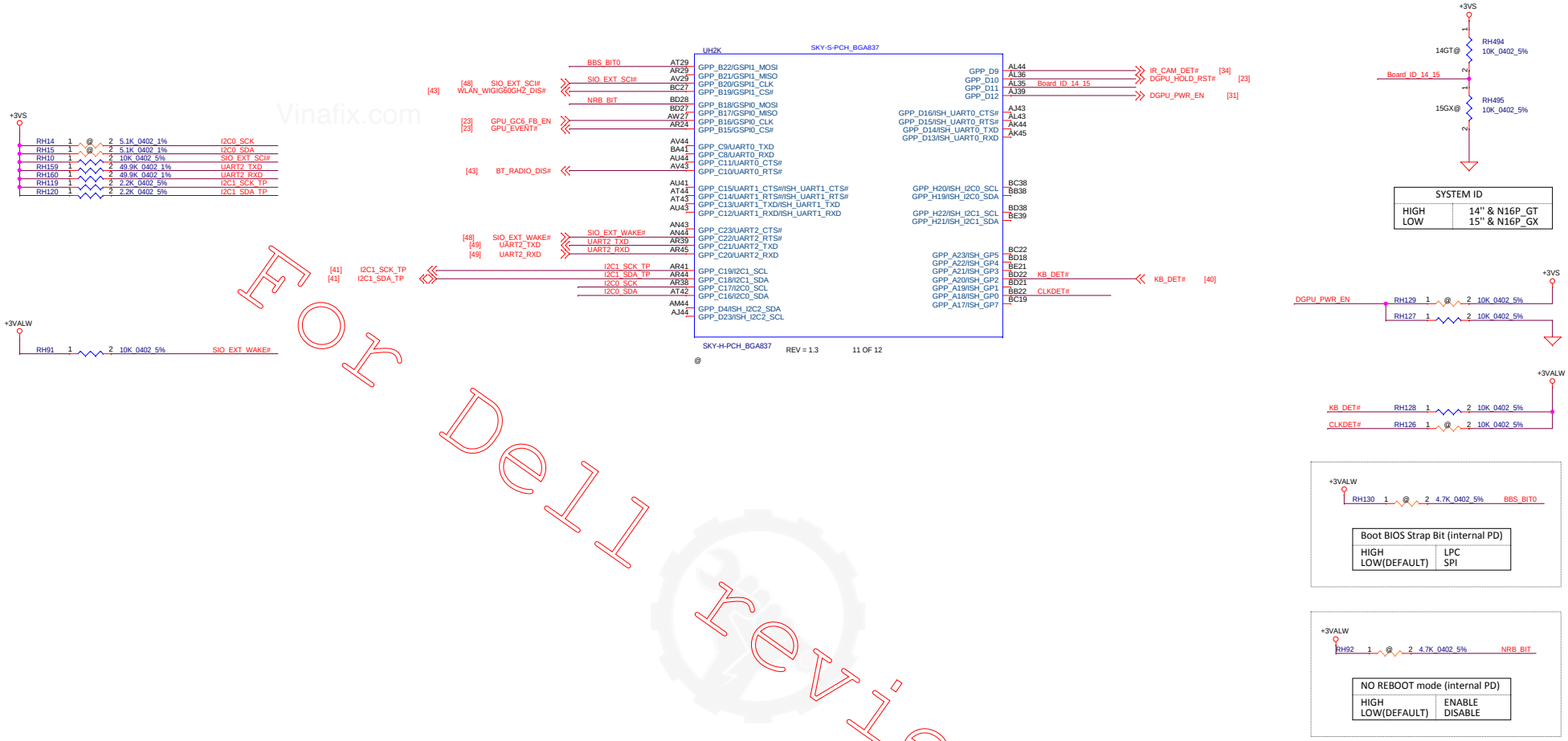
Title: **PCH (4/8) PCI, USB**

Size: | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 19 of 70



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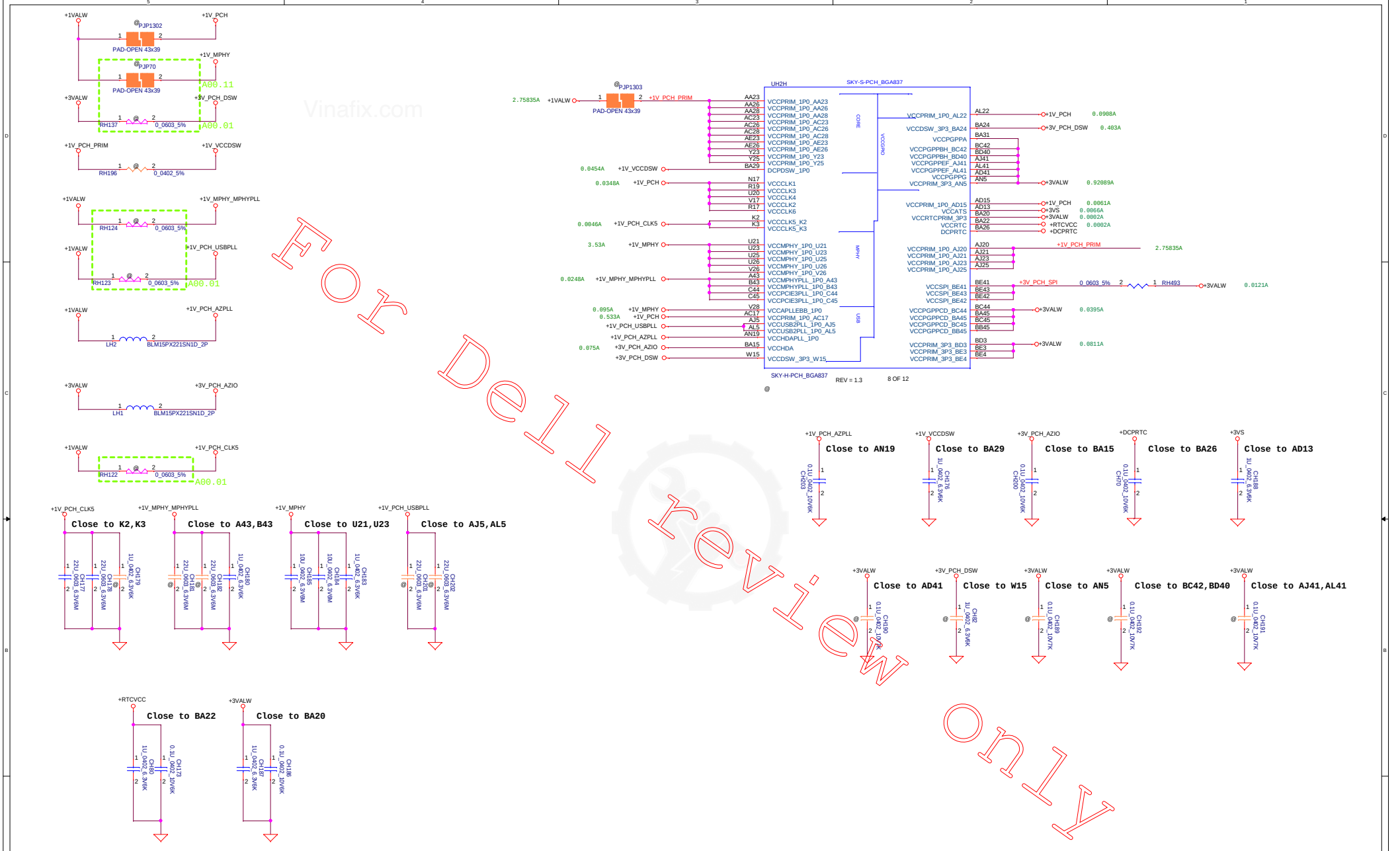
Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 20 of 70



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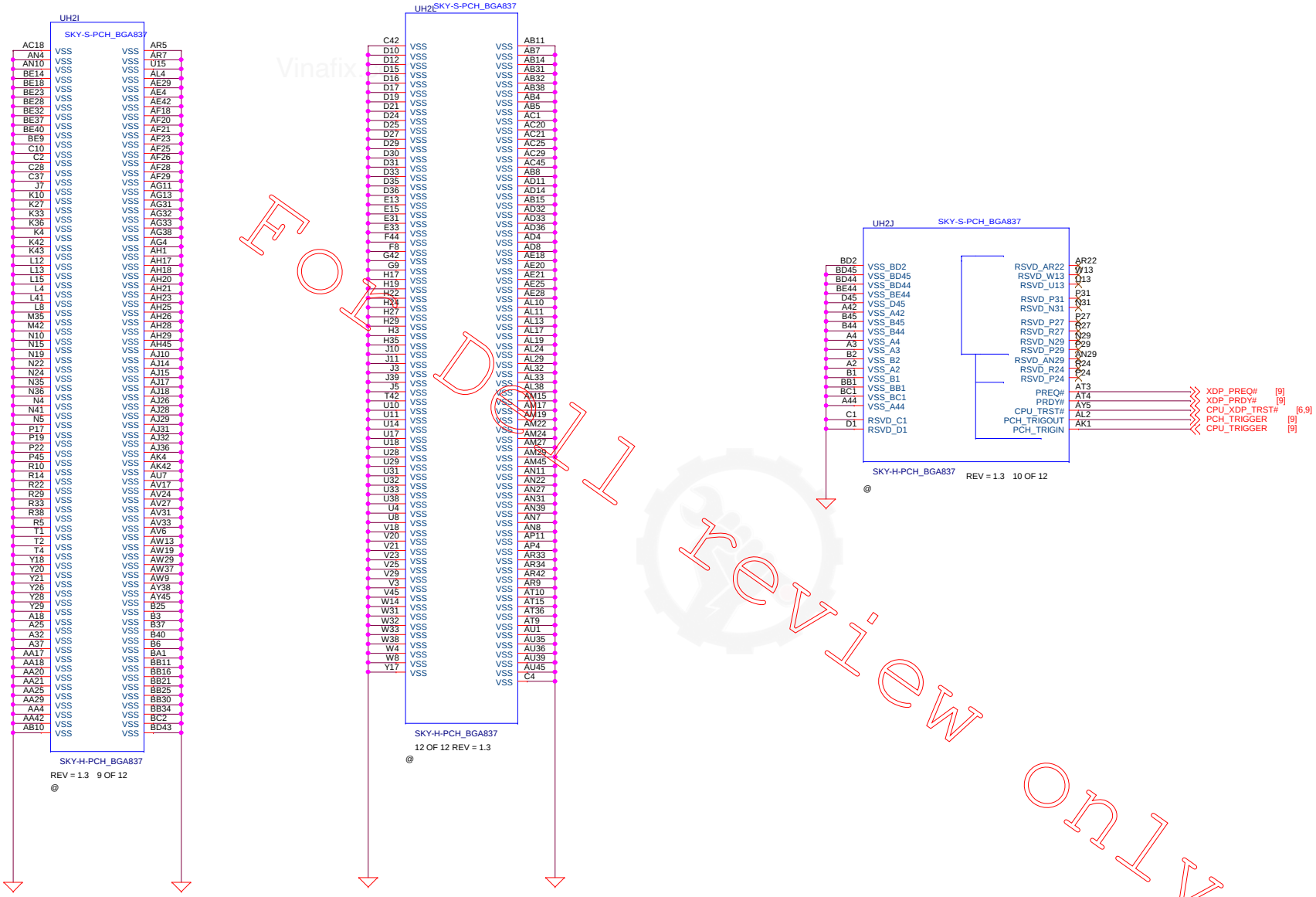
Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 21 of 70



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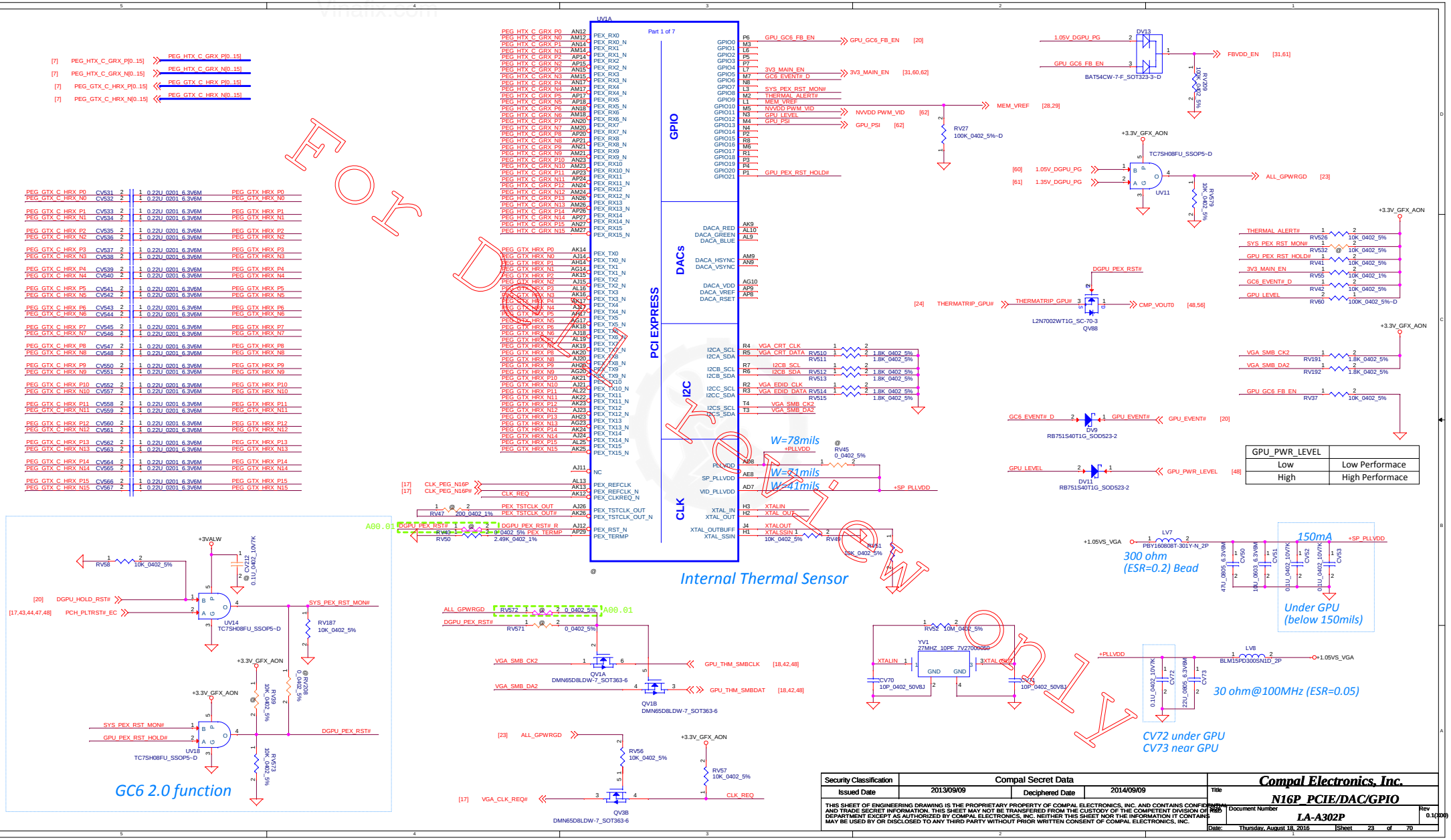
Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Document Number: **LA-D991P**

Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 22 of 70



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Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title: N16P_PCIE/DAC/GPIO
				Document Number: LA-A302P
				Rev: 0.1(100)
Date: Thursday, August 18, 2016		Sheet 23 of 70		

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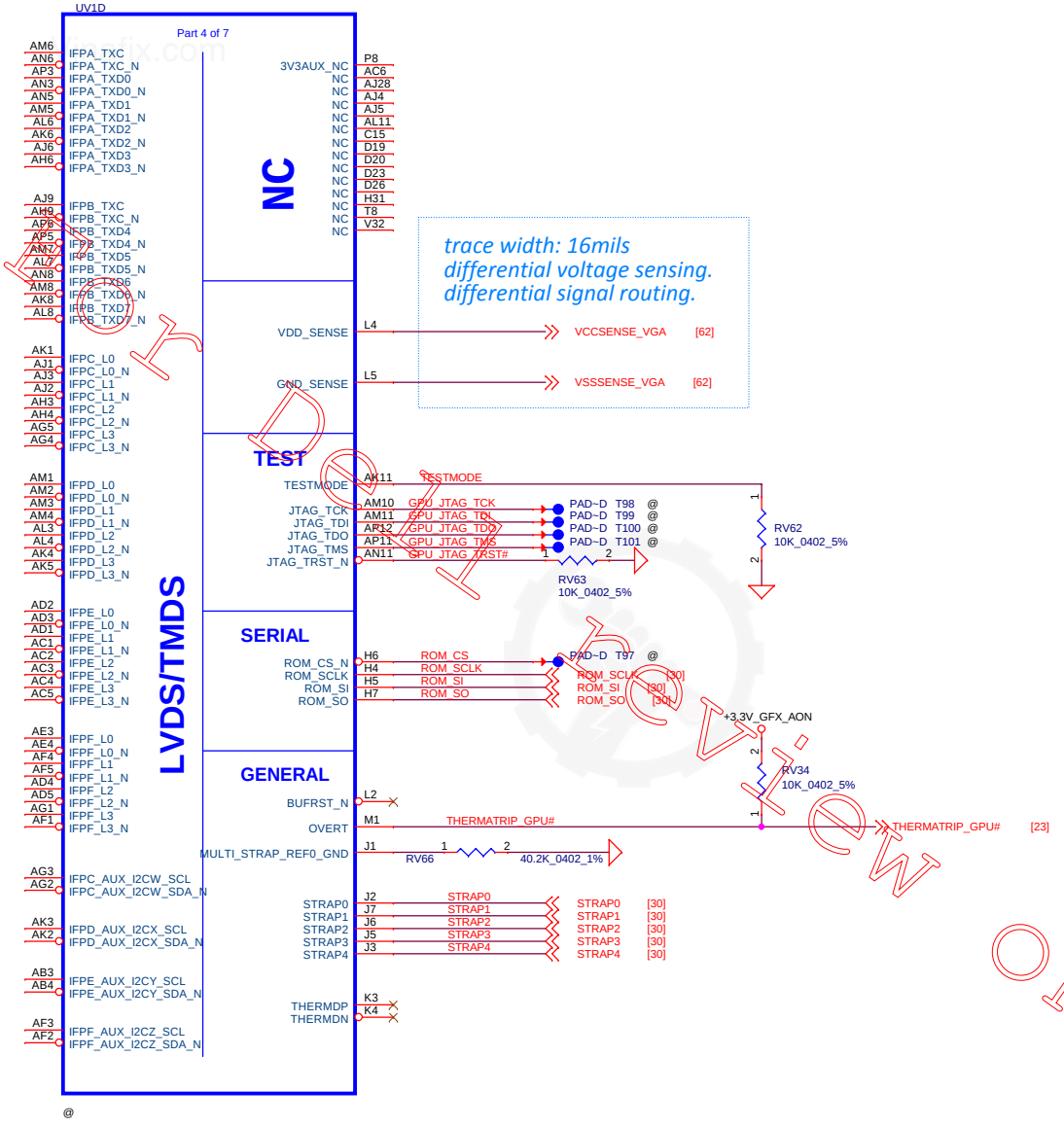

trace width: 16mils
differential voltage sensing.
differential signal routing.

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Issued Date	2013/09/09	Deciphered Date	2014/09/09

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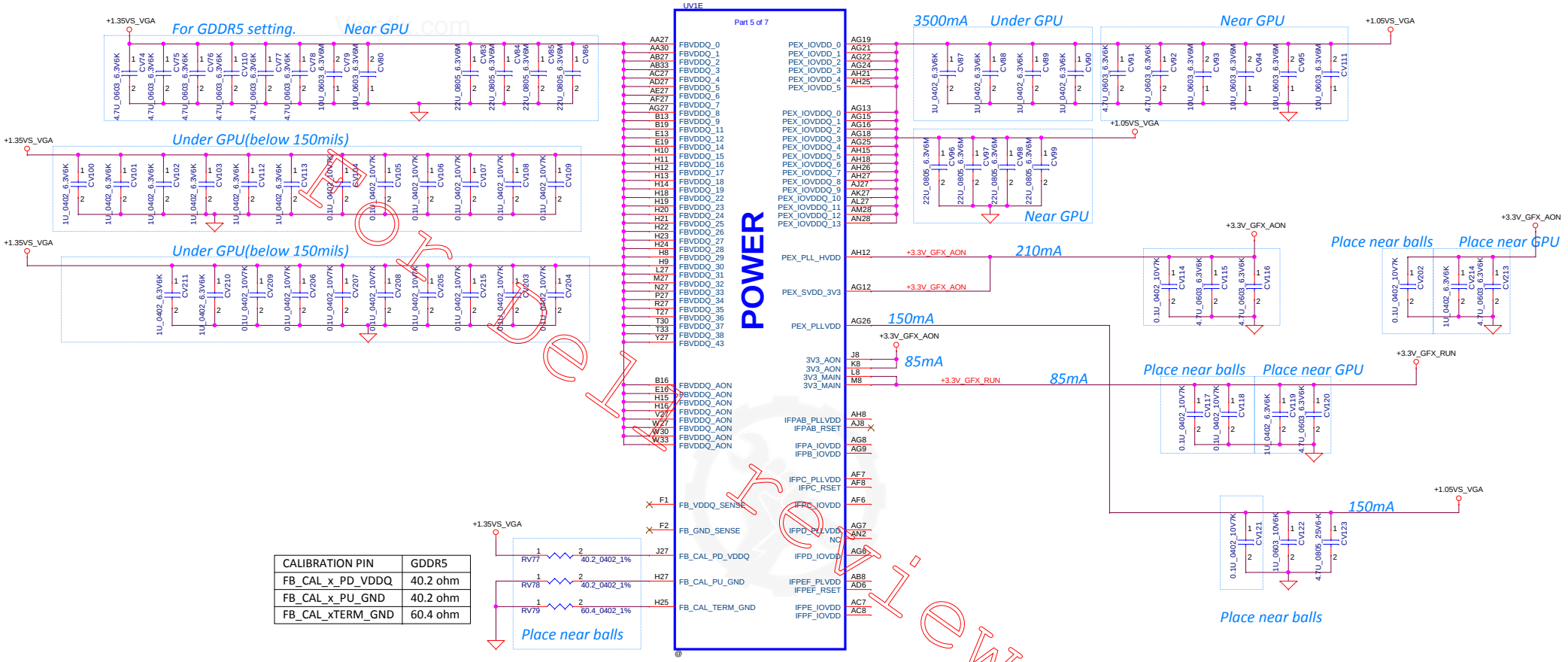
Compal Electronics, Inc.

Title: **N16P_eDP/HDMI/mDP**

Size | Document Number: **LA-A302P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 24 of 70



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

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Compal Electronics, Inc.

Title: **N16P_Power**

Document Number: **LA-A302P**

Rev: 0.1(100)

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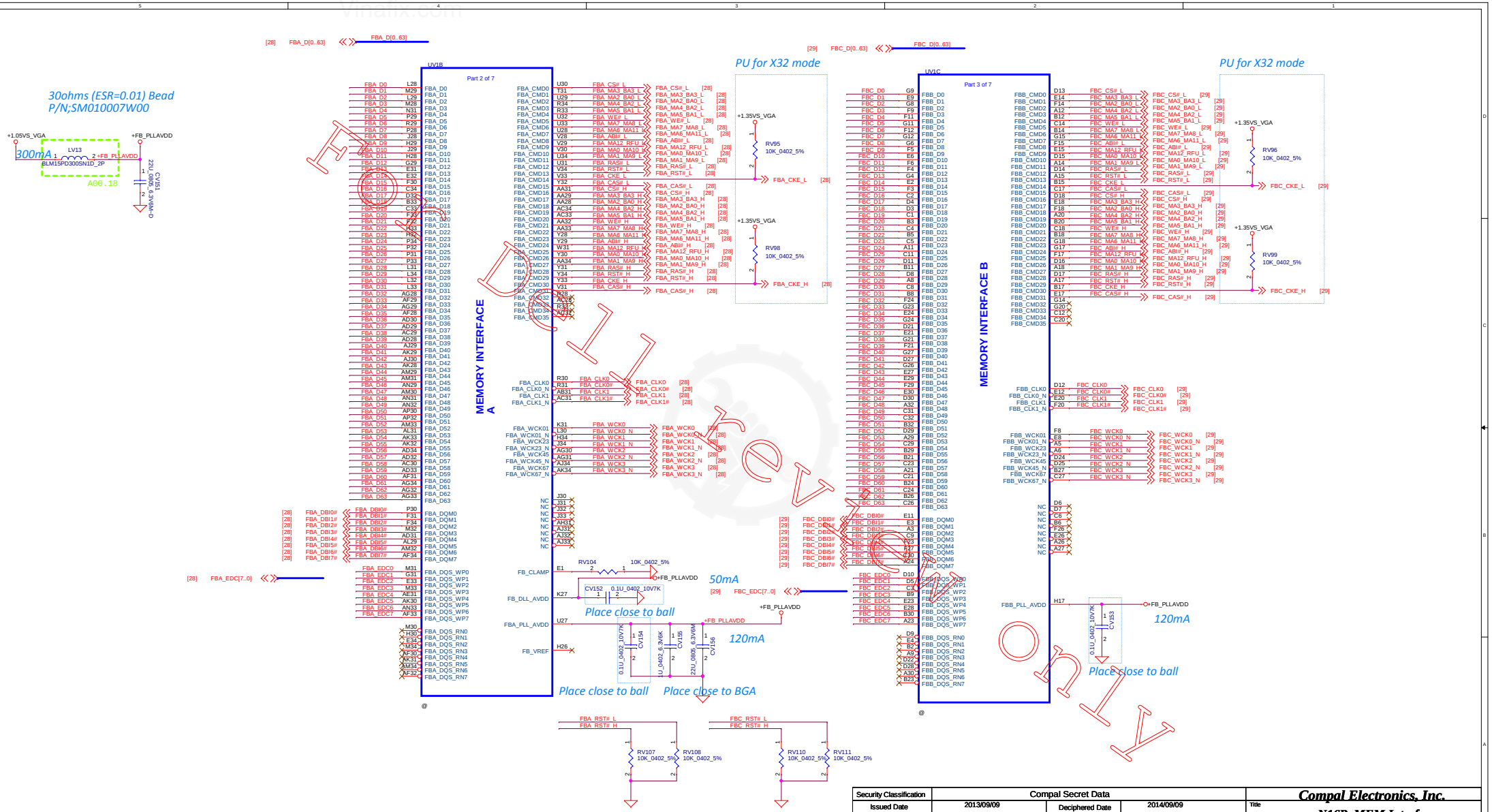
Compal Electronics, Inc.

Title: **N16P_VGA CORE/GND**

Size: | Document Number: **LA-A302P** | Rev: 0.1(000)

Date: Thursday, August 18, 2016 | Sheet 26 of 70



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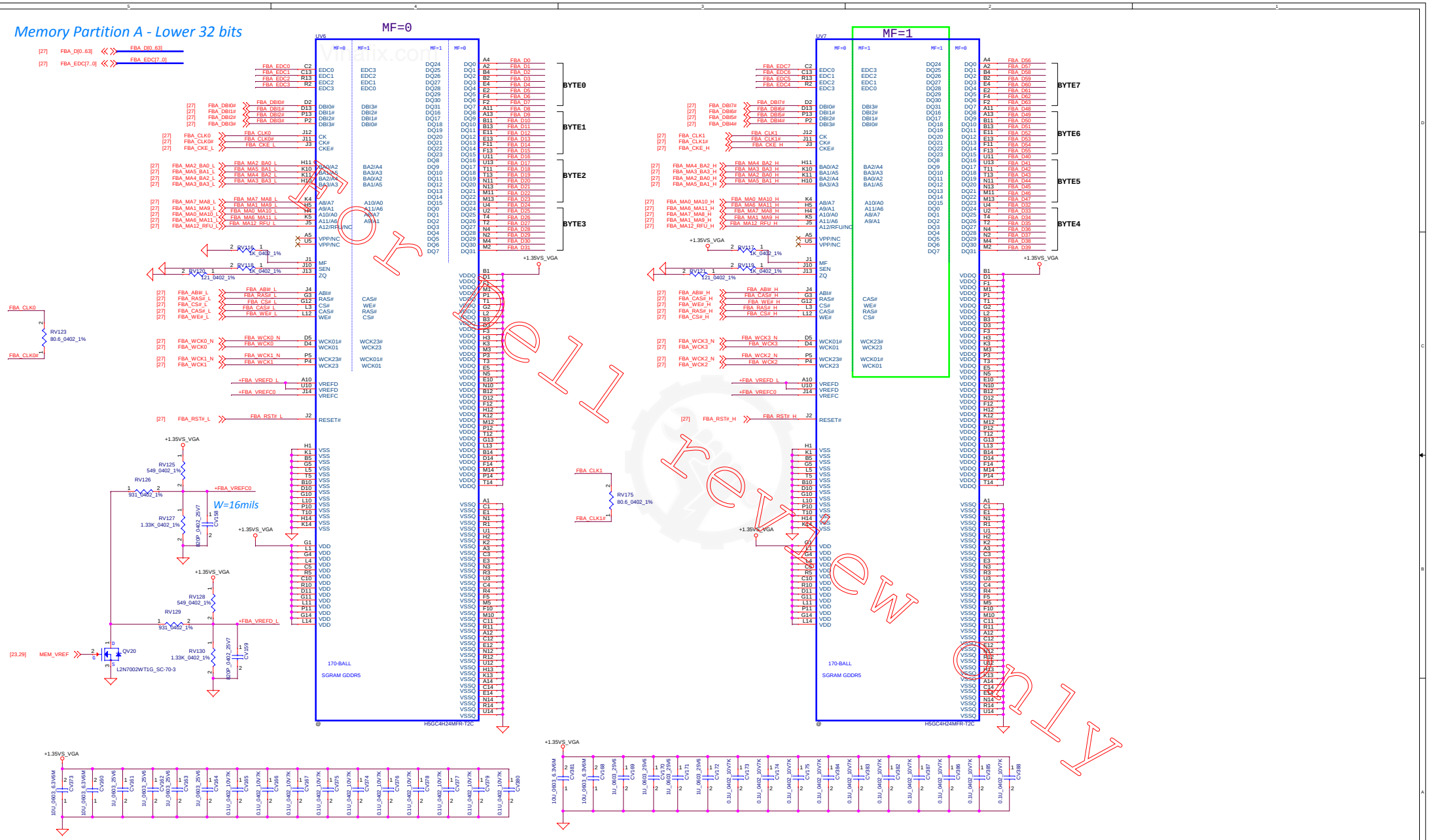
Compal Electronics, Inc.

Title: **N16P_MEM Interface**

Document Number: **LA-A302P** Rev: 0.1(100)

Date: Thursday, August 18, 2016 Sheet 27 of 70



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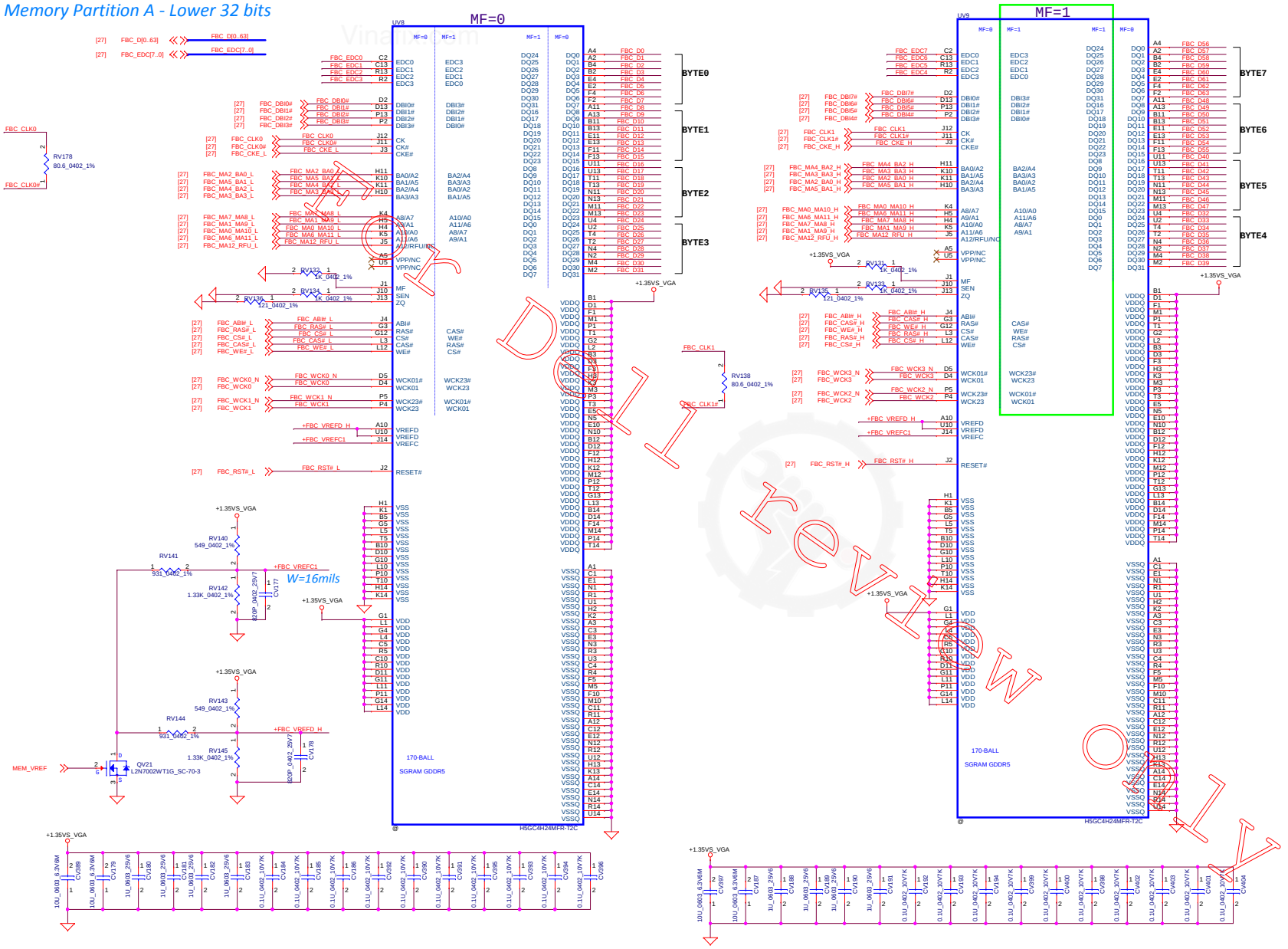
Title: N16P GDDR5 A

Size: | Document Number: LA-A302P | Rev: 0.1(0.00)

Date: Thursday, August 18, 2016 | Sheet 28 of 70

Memory Partition A - Lower 32 bits



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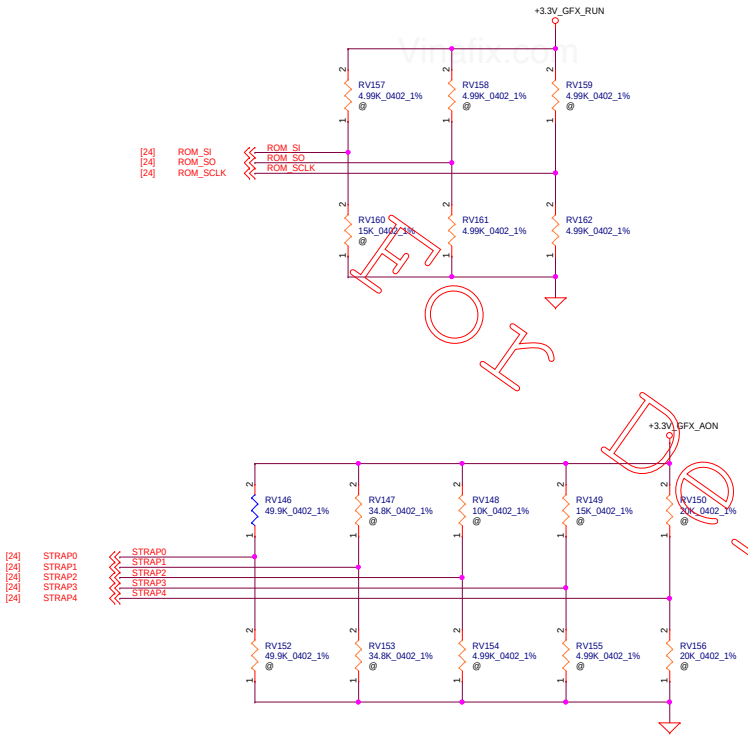
Compal Electronics, Inc.

Title: **N16P GDDR5 B**

Size: | Document Number: **LA-A302P** | Rev: 0.1(0.00)

Date: Thursday, August 18, 2016 | Sheet 29 of 70



4Gb G5	Vendor PN	Die Revision	Strap
Hynix	H5GC4H24AJR-R0C	A-die	0x6
Micron	EDW4032BABG-70-F	A-die	0x4
8Gb G5	**Vendor PN**	**Die Revision**	**Strap**
Samsung	K4G80325FB-HC28	B-die	0x8
Micron	MT51J256M32HF-70:A	A-die	0x9

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

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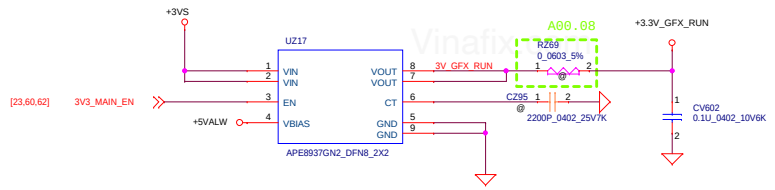
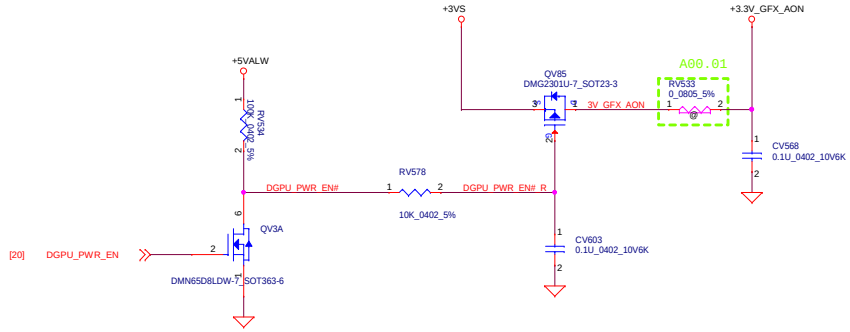
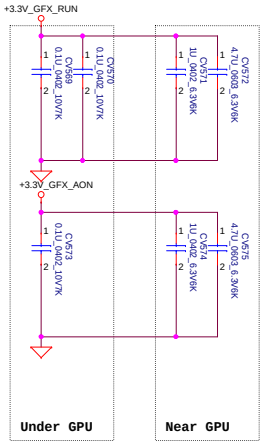
+3.3V_GFX_RUN



+3VALW to +3.3V_GFX_AON

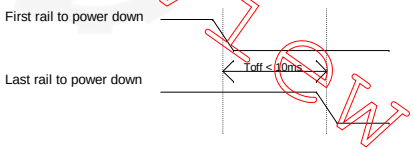




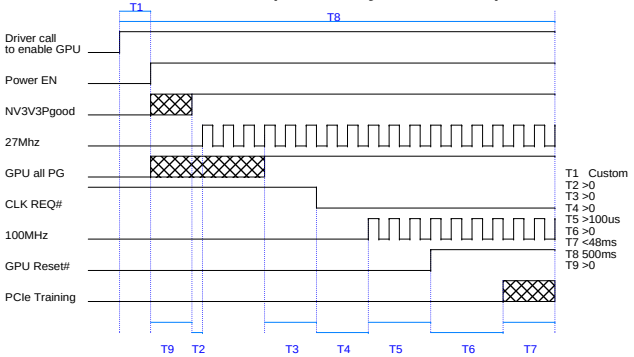
GPU Power Up Power Rail Sequence

The ramp time for any rail must be more than 40us.

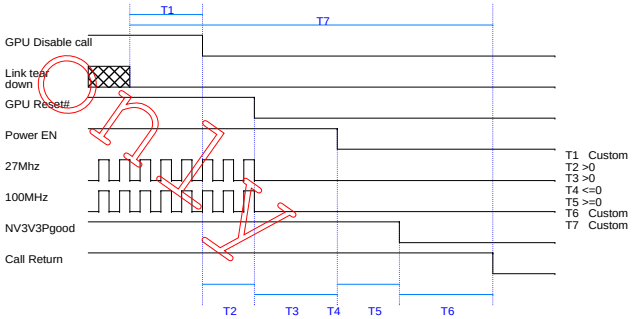
GPU Power Down Sequence



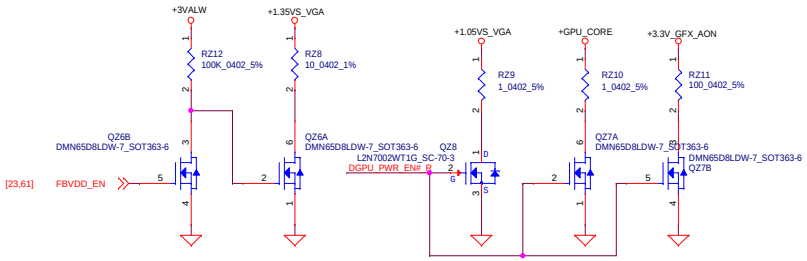
GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Discharge



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Title: **GPU DC/DC interface**

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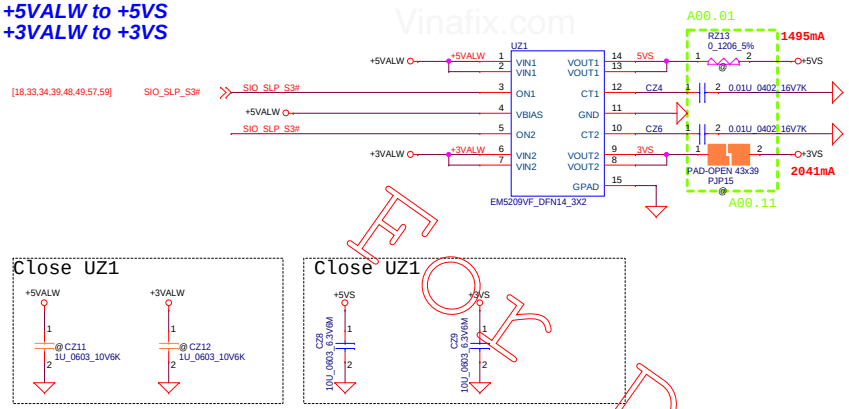
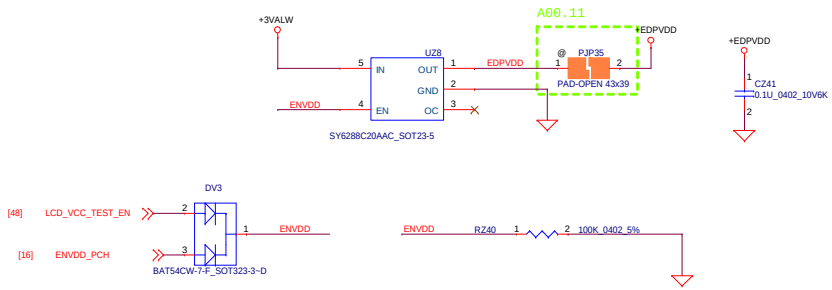
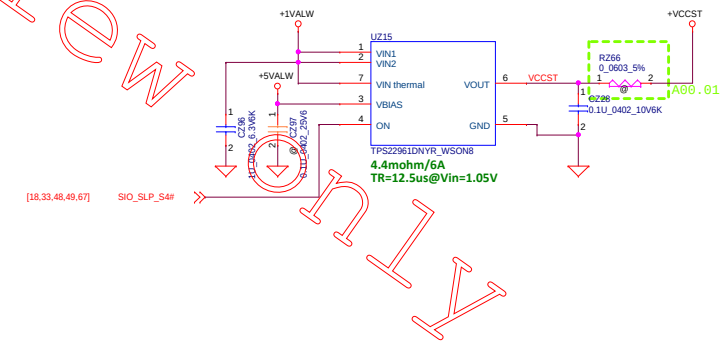
+5VALW to +5VS
+3VALW to +3VS



eDP & Camera Load Switch



+VCCST Load Switch



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Compal Electronics, Inc.

Title: **SYS DC/DC Interface**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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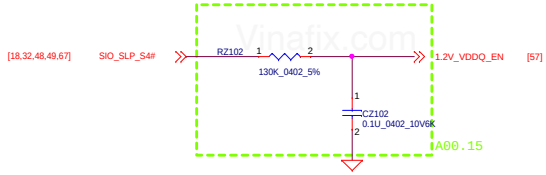
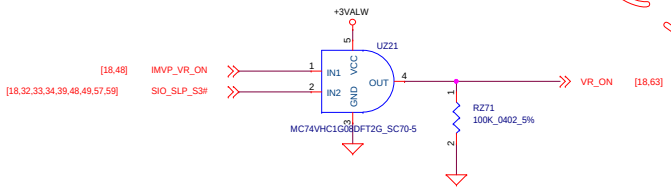
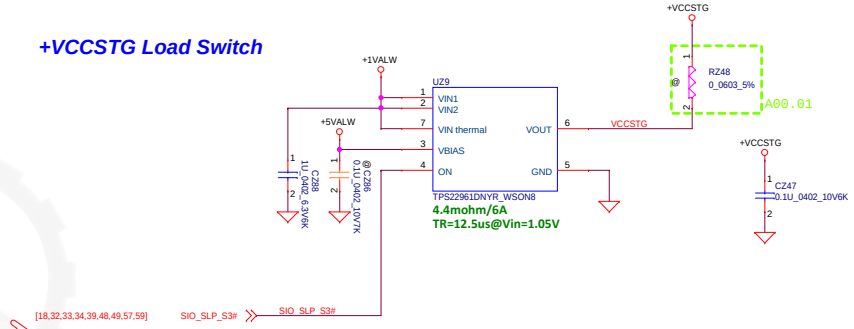
+1.2V_DDR Enable

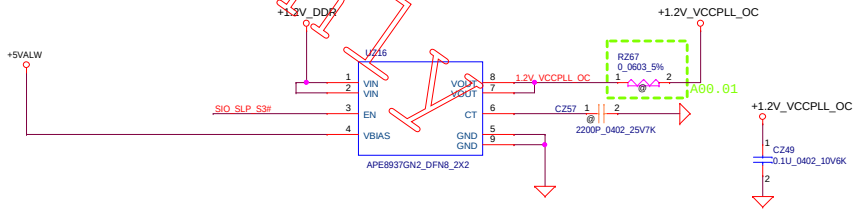




+VCCSTG Load Switch



+VCCPLL_OC Load Switch



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Title: **EC ENE-KB9012/ KC3810**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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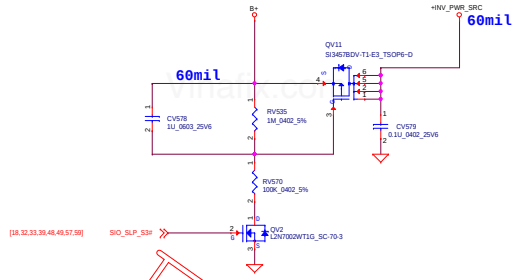
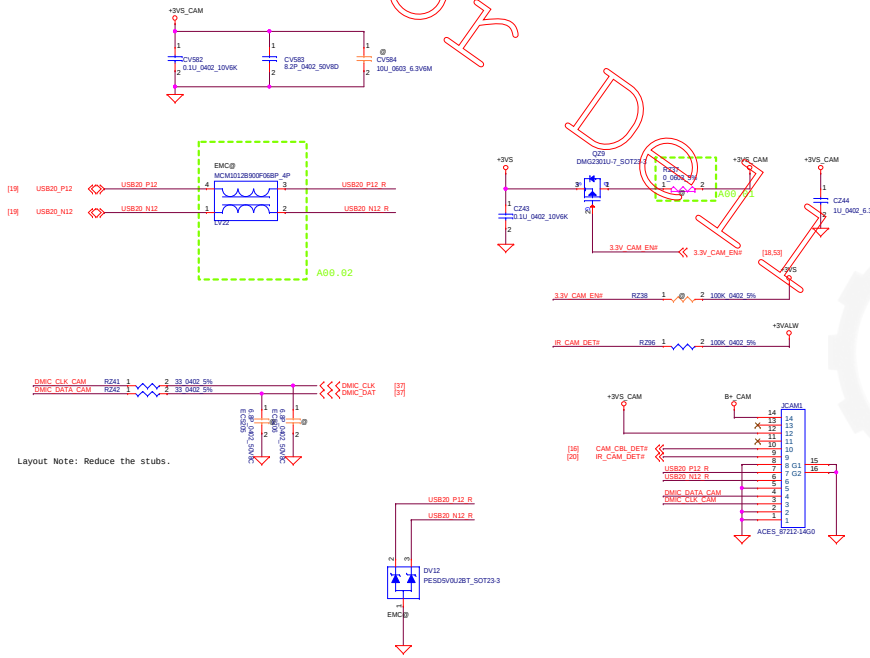
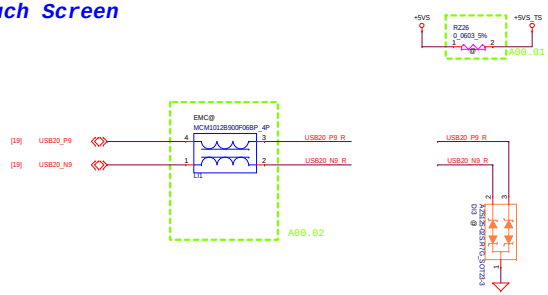
LCD backlight PWR CTRL



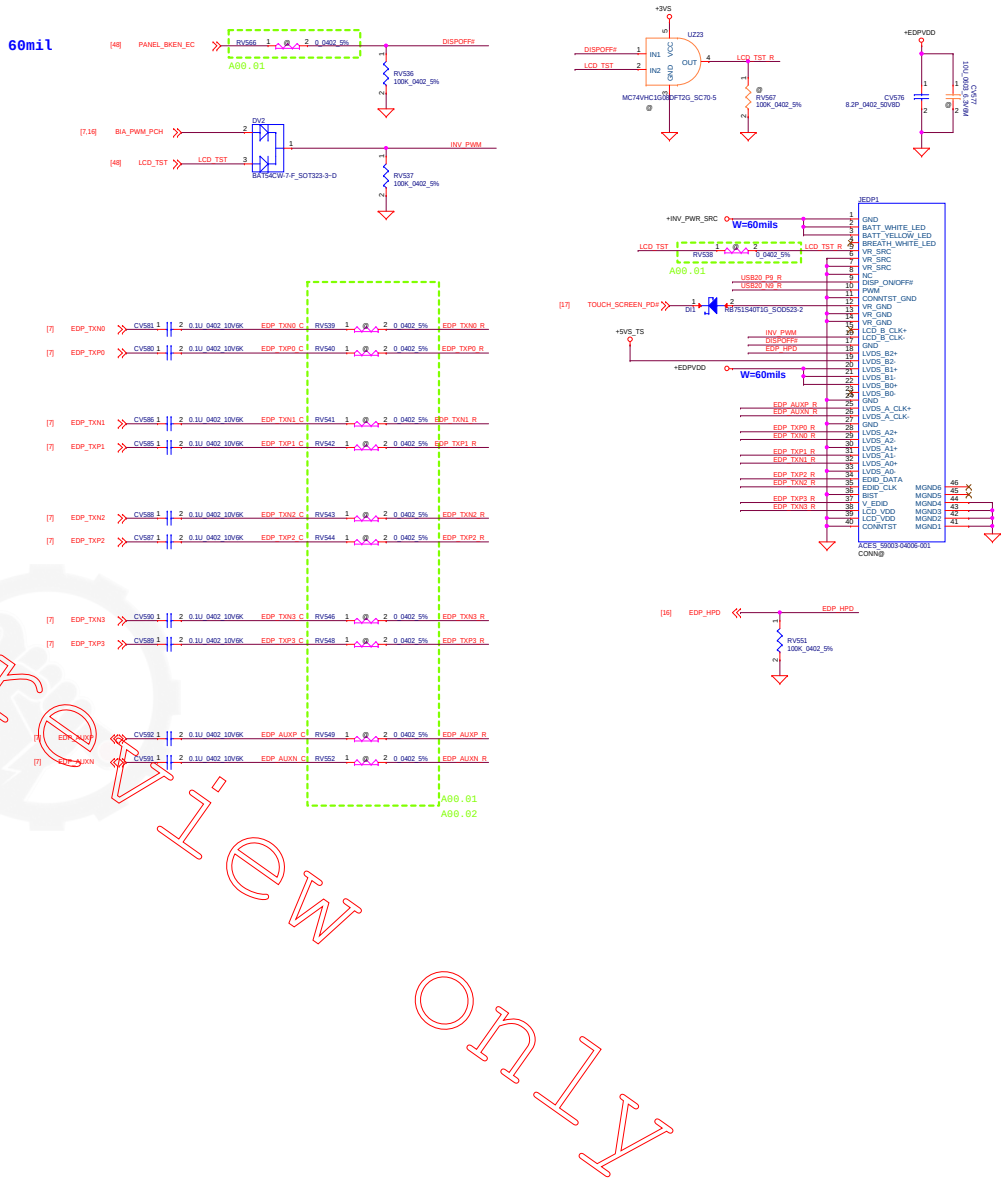
CCD +DMIC Conn.



Touch Screen



eDP & TS Conn.



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				Size: A; Document Number: LA-D991P; Rev: 0.1(0.0)
				Date: Thursday, August 18, 2016; Sheet 34 of 70

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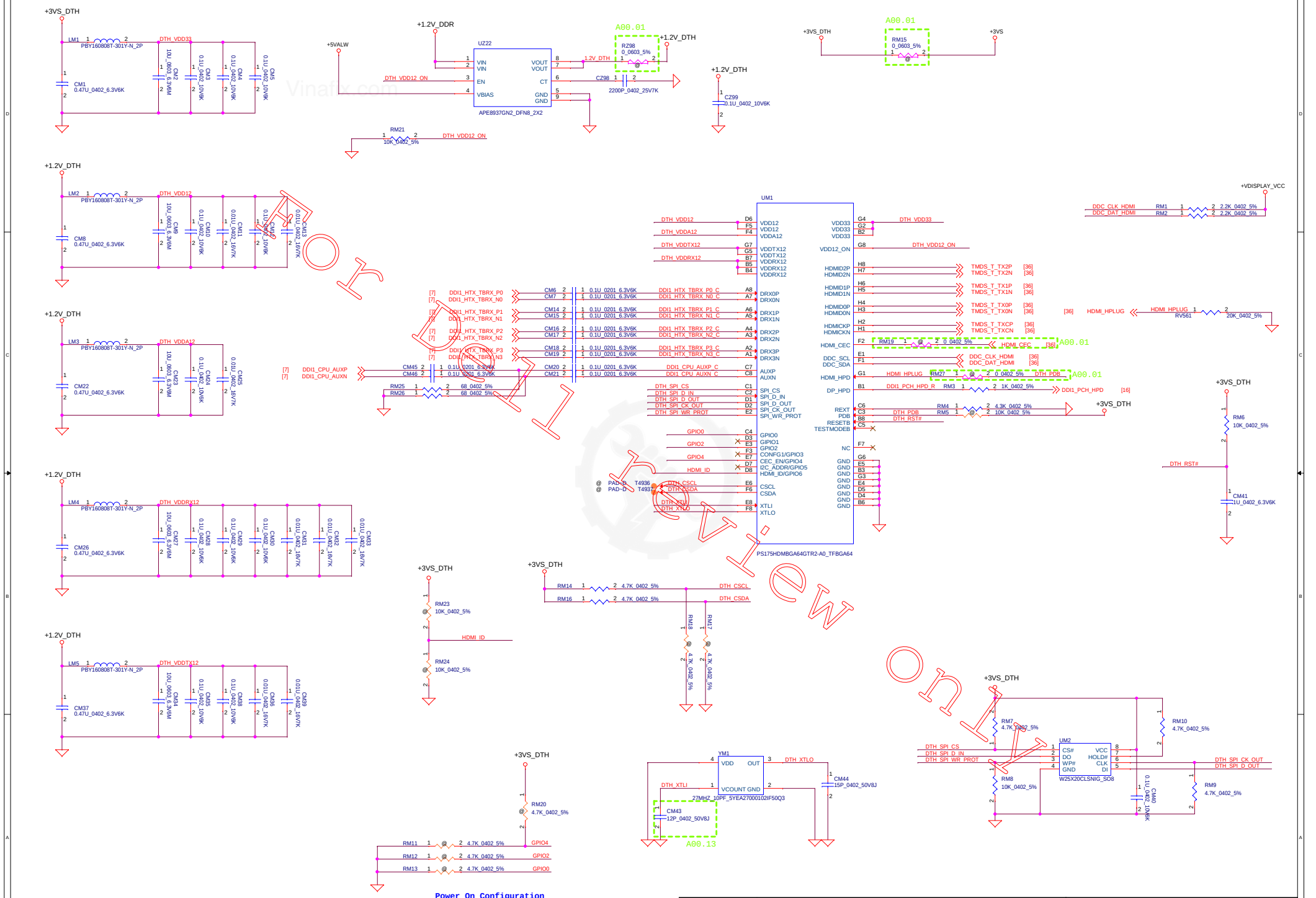

Power On Configuration

GPIO2:Firmware initial address, internal pull-up~80K
0: Start from Bank 7 1: Start from Bank 3 (default)

GPIO0 : Pre-emphasis setting; Internal pull up
1:default, no pre-emphasis 0:pre-emphasis=2.5dB

CEC_EN/GPIO4: For debug purpose

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

Size: C | Document Number: LA-C361P | Rev: 0.1(X00)

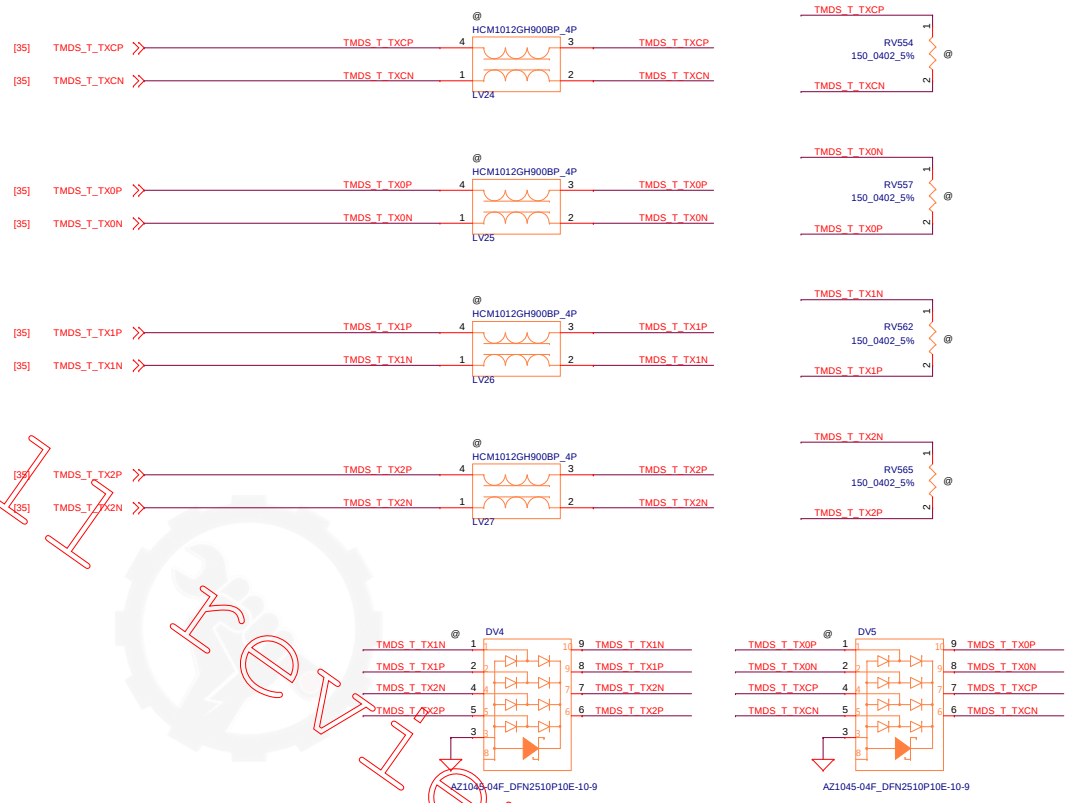
Date: Thursday, August 18, 2016 | Sheet 35 of 70

Vinafix.com

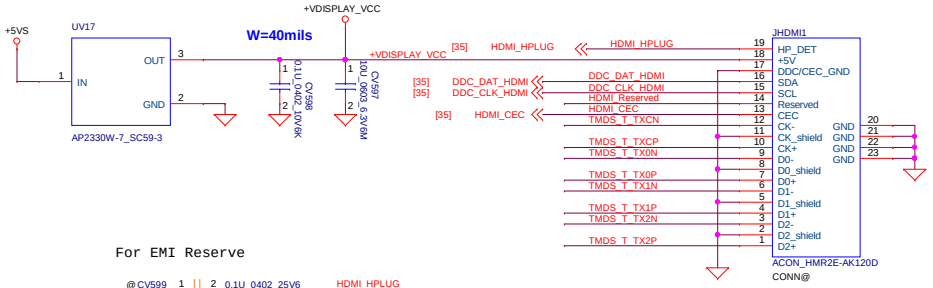
For Deep review only

Place close to JHDMI1

Place between ESD and CM-Choke



HDMI conn



For EMI Reserve

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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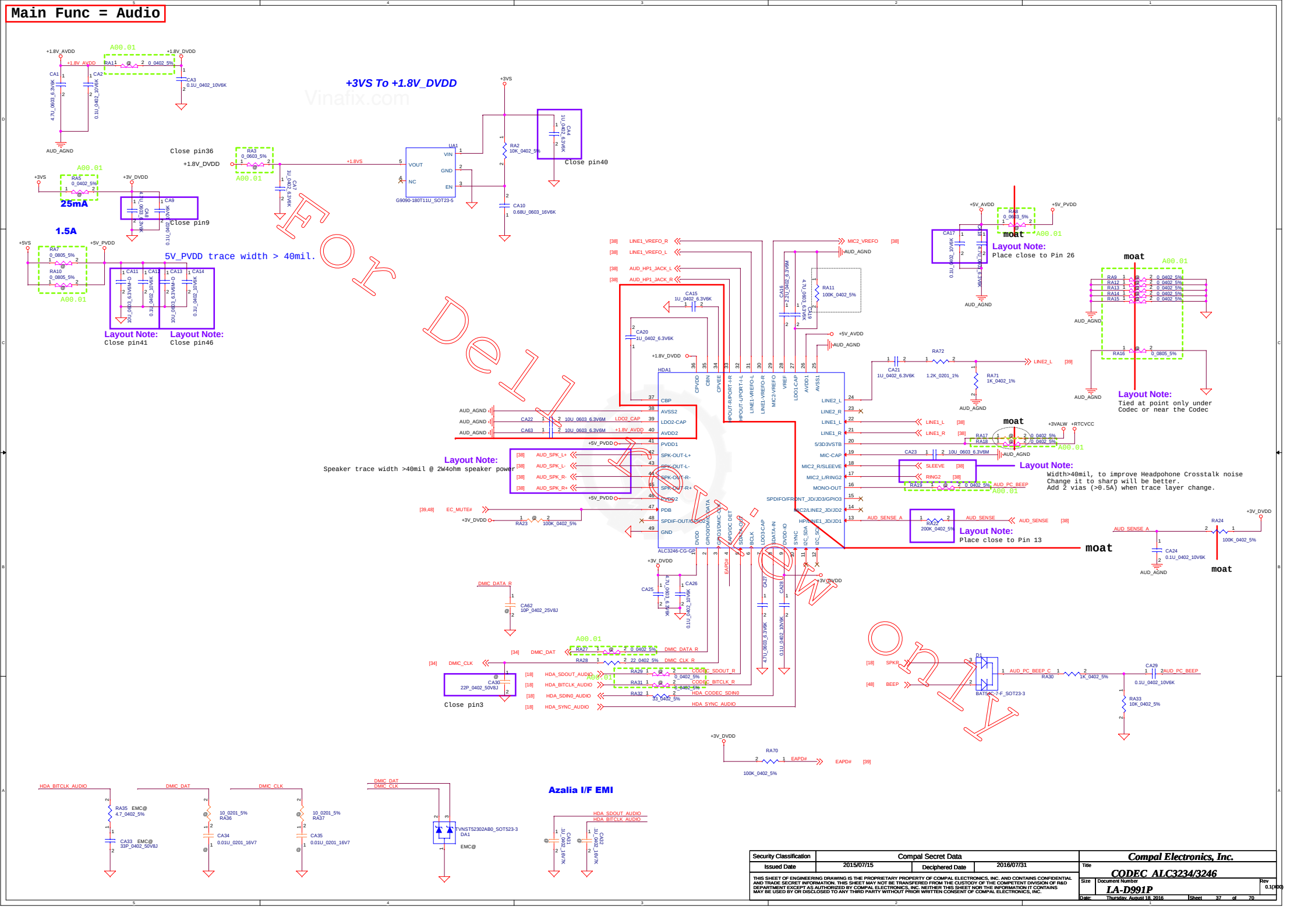
Compal Electronics, Inc.

Title: **HDMI**

Size: Custom | Document Number: LA-C361P | Rev: 0.1(000)

Date: Thursday, August 18, 2016 | Sheet 36 of 70

Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

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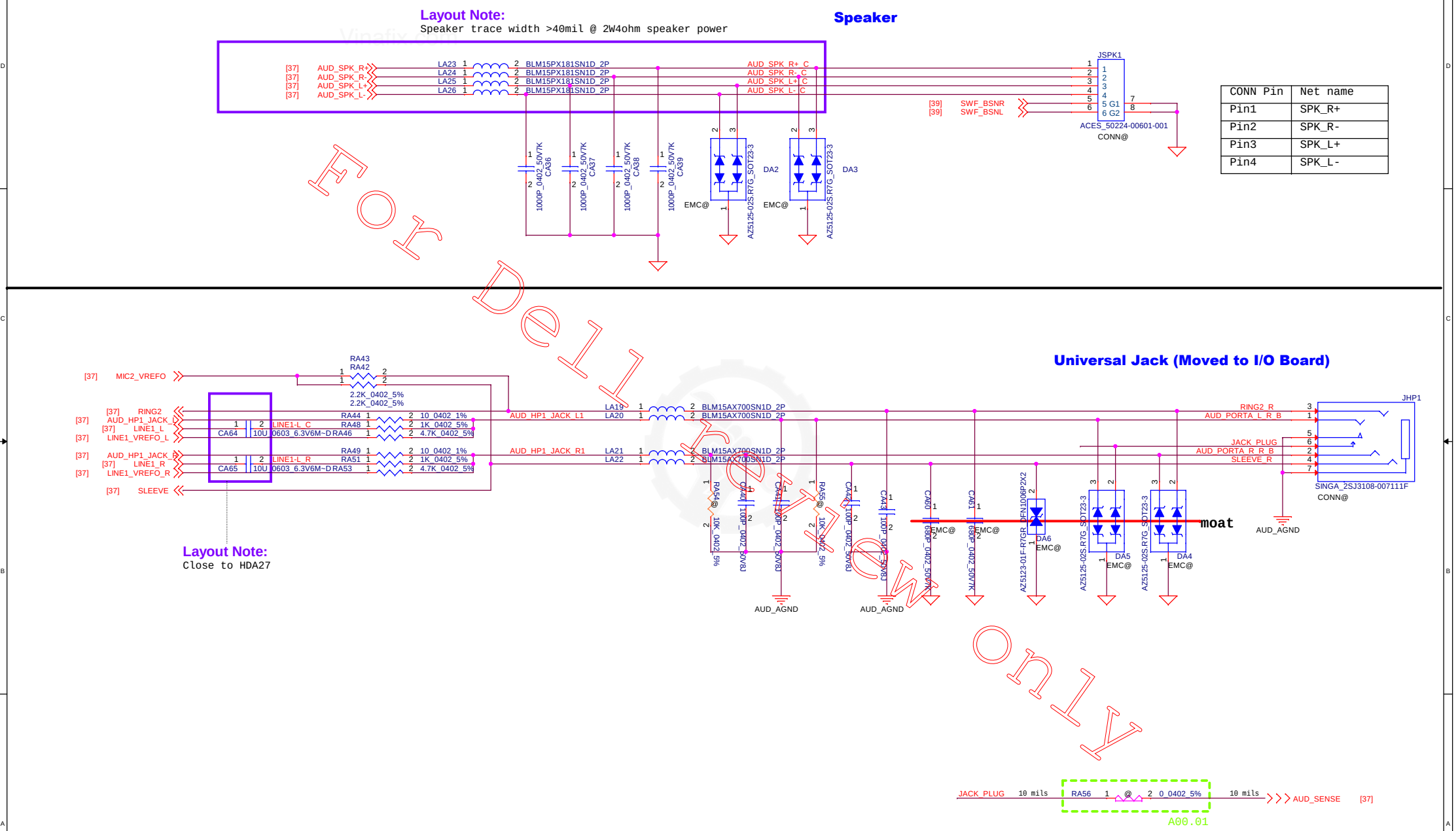
Compal Electronics, Inc.

Title: **CODEC ALC3234/3246**

Size: | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 37 of 70

Main Func = Audio



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

For Deliberation Only

Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

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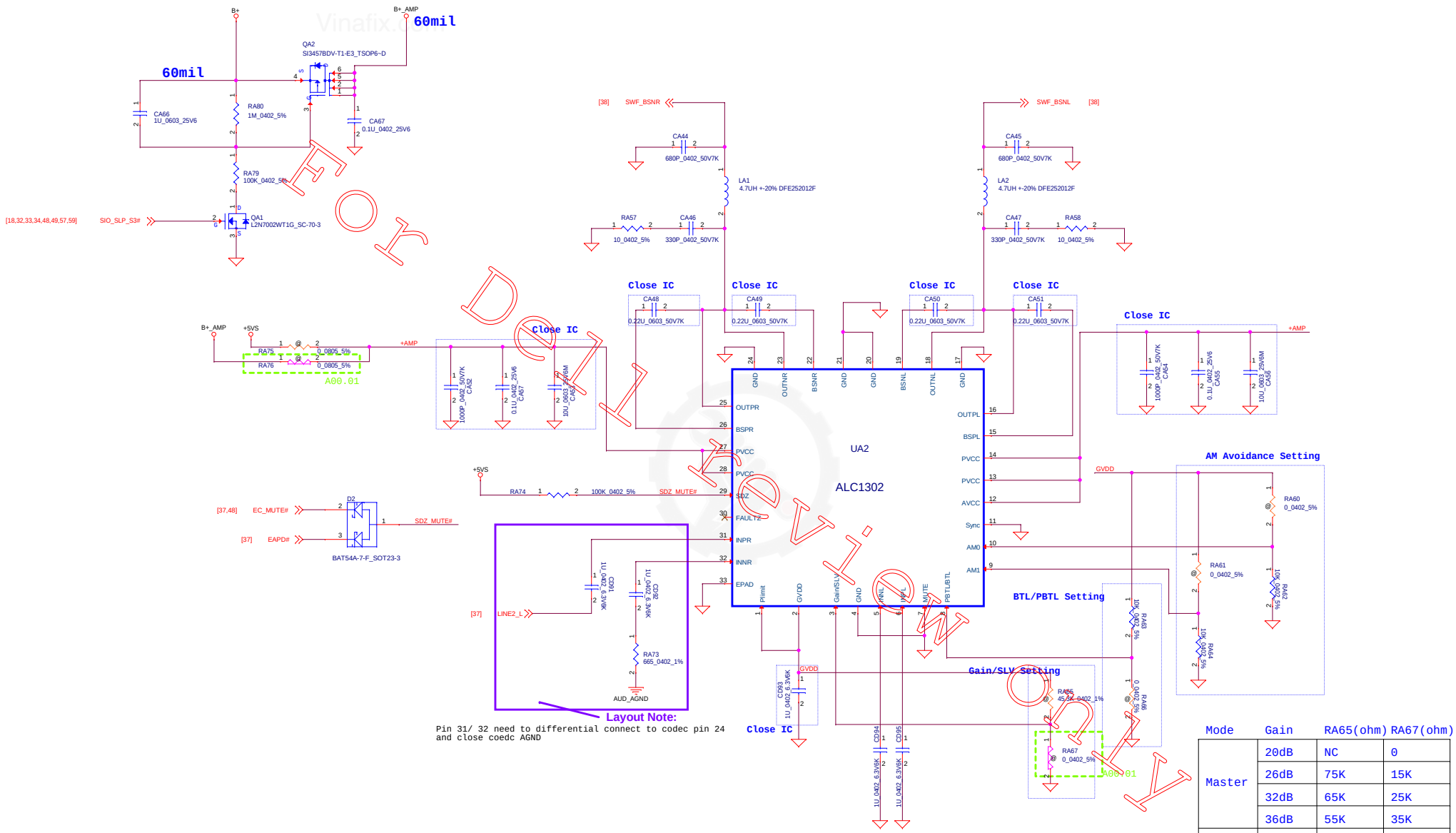
Compal Electronics, Inc.

Title: **SPKR/JACK**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 38 of 70

Subwoofer AMP



Mode	Gain	RA65(ohm)	RA67(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC

Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: P3-SMART AMP

Size | Document Number: LA-D991P | Rev: 0.1(XXX)

Date: Thursday, August 18, 2016 | Sheet 39 of 70

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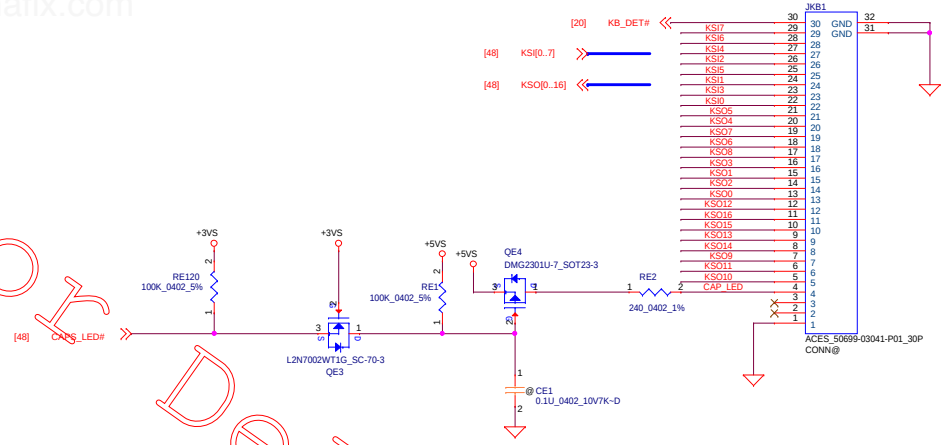
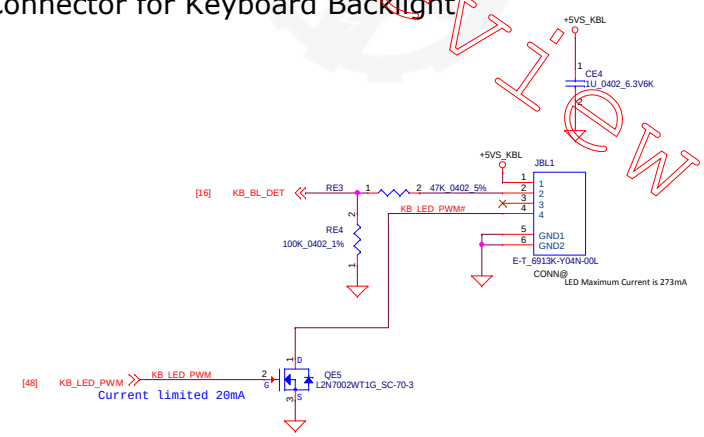
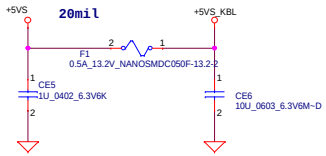
Connector for Keyboard



Connector for Keyboard Backlight



Fuse for Backlight



For Dell review only

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title: P03-KB Controller
				Size / Document Number: LA-D991P / Rev: 0.1(X00)
				Date: Thursday, August 18, 2016 / Sheet 40 of 70

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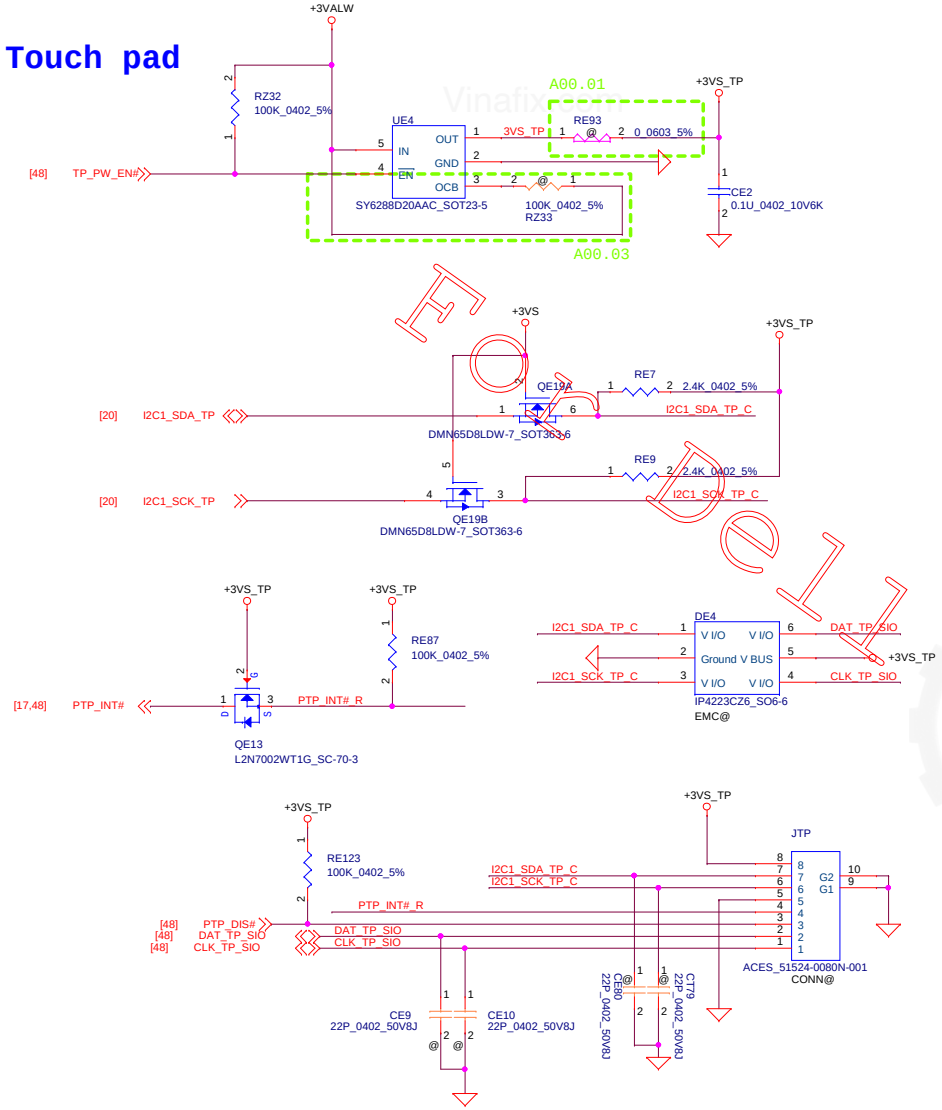
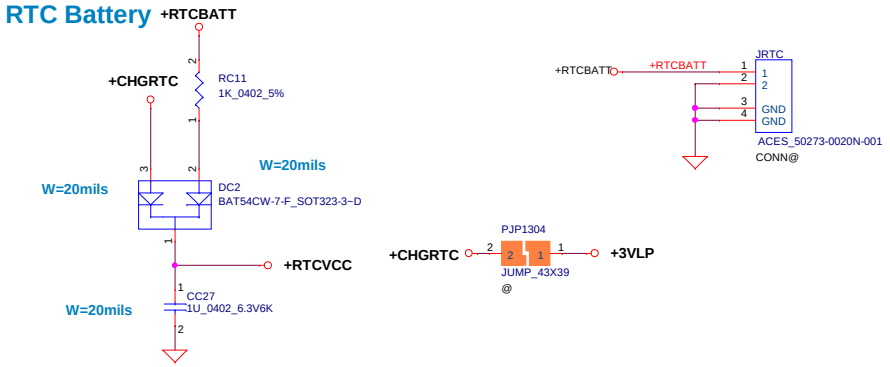
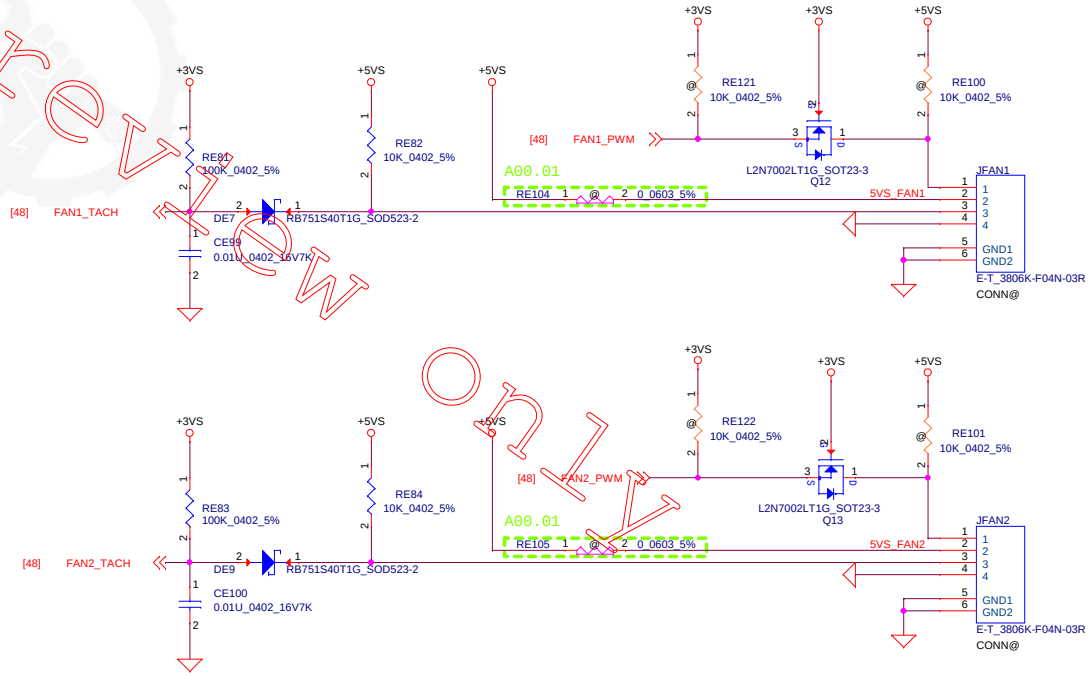
Touch pad



RTC Battery non- Charge Function



PWM FAN



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: FAN/TP/KB/PWR SW

Size: Custom | Document Number: LA-D991P | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 41 of 70

Main Func : Fan/Thermal

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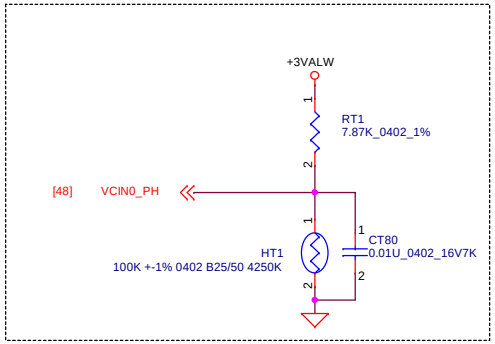
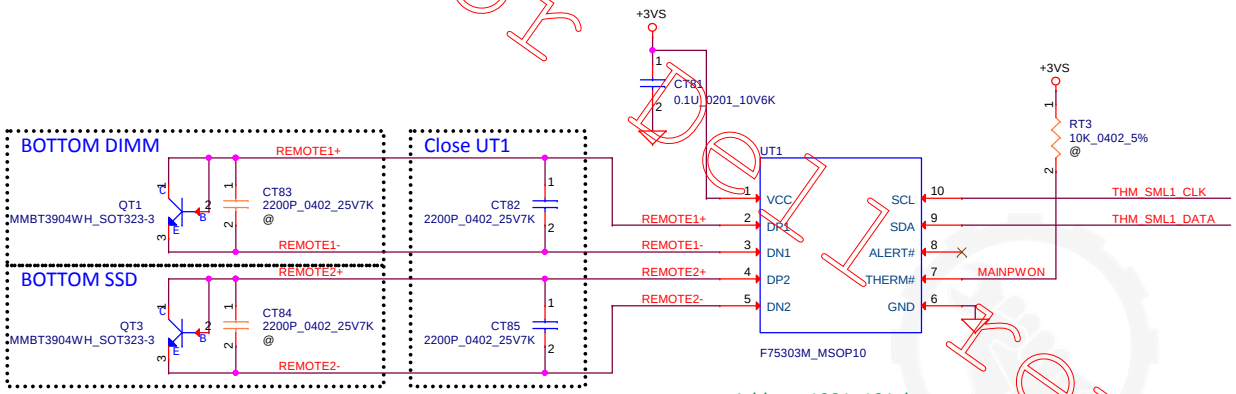
CPU TOP side



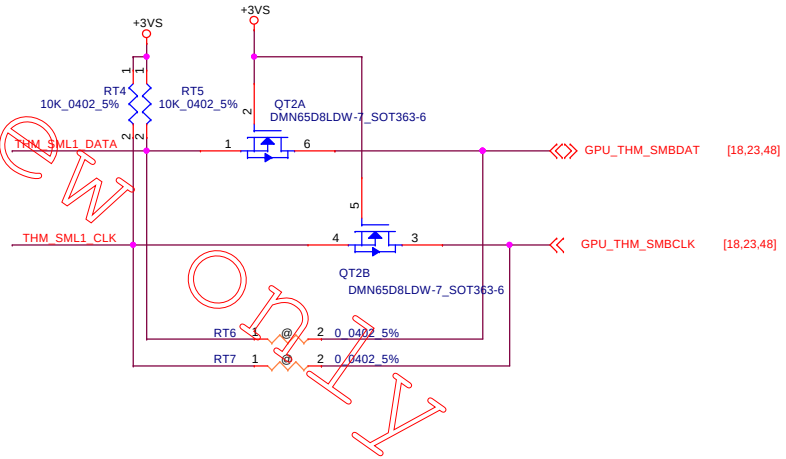
Fintek thermal sensor placed TOP near between GPU & CPU



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR



Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

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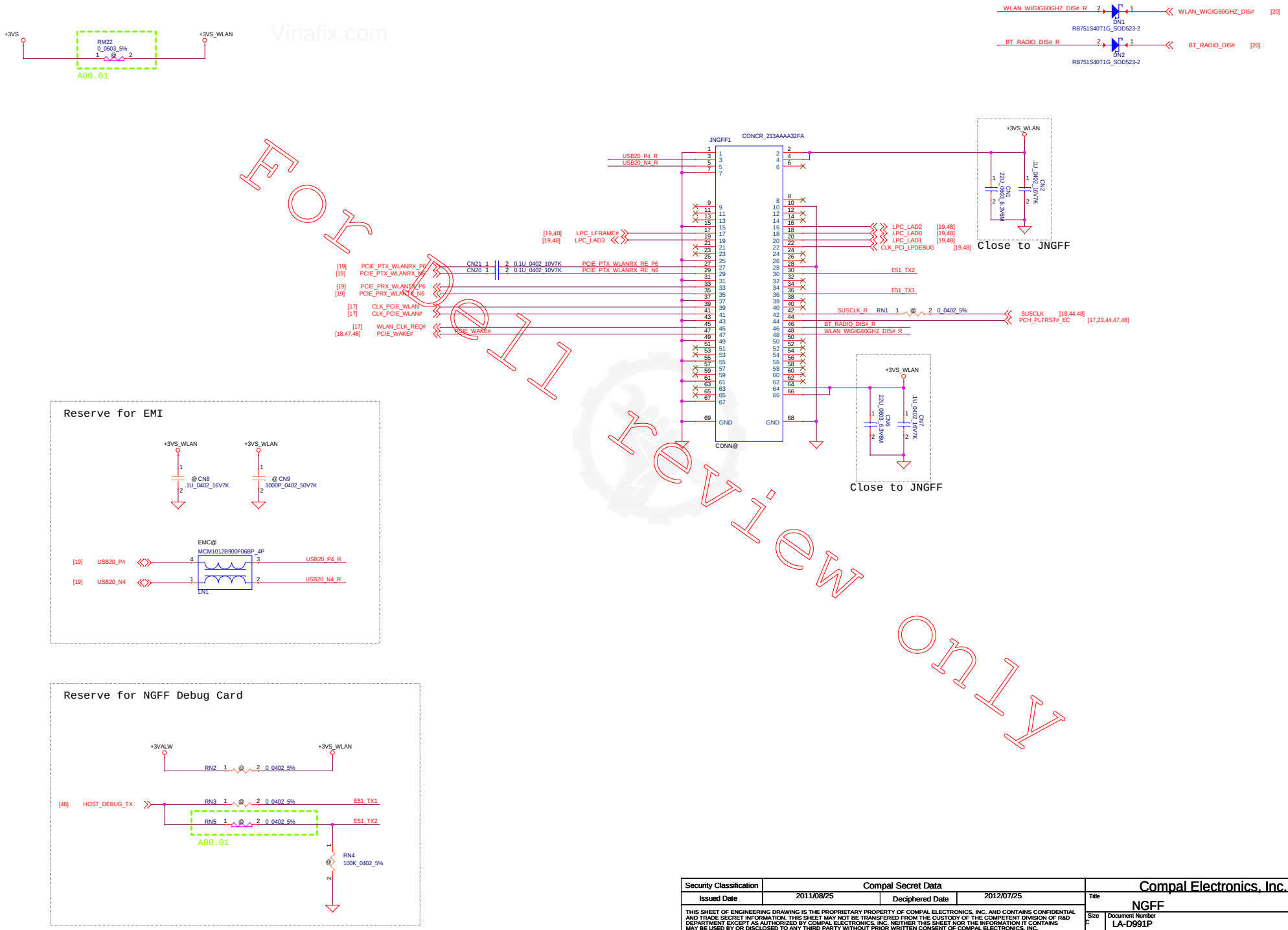
Compal Electronics, Inc.

Title: **Thermal Sensor**

Size | Document Number: **LA-D991P** | Rev: 0.1(0.00)

Date: Thursday, August 18, 2016 | Sheet 42 of 70

M.2 Slot-A Key-A (WLAN + BT)



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Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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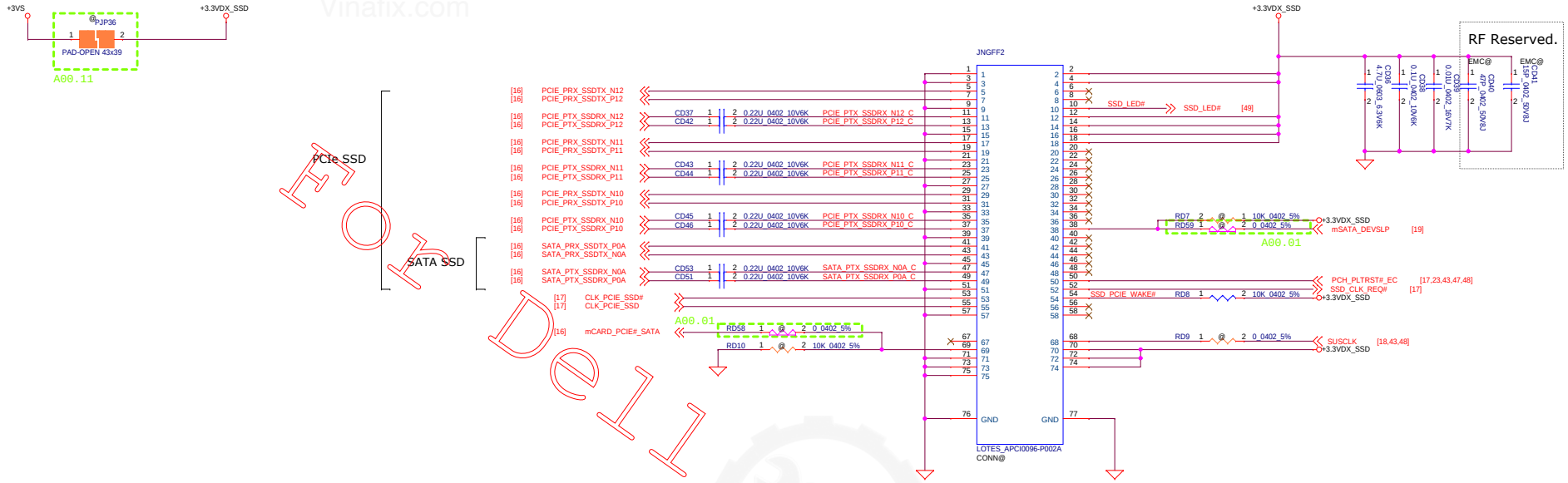
Compal Electronics, Inc.

Title: NGFF

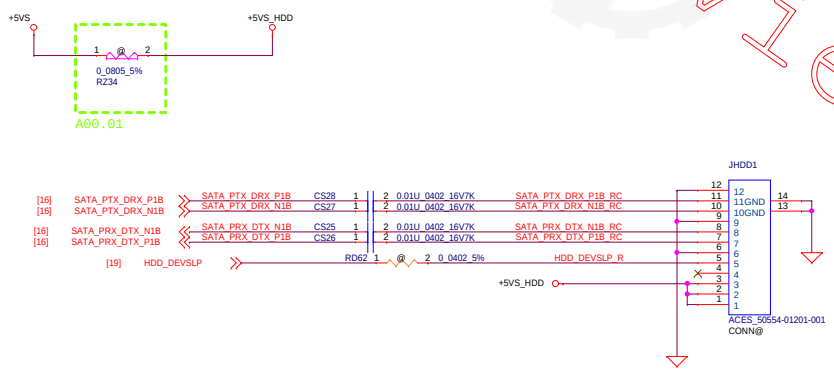
Size: C | Document Number: LA-D991P | Rev: 0.1(000)

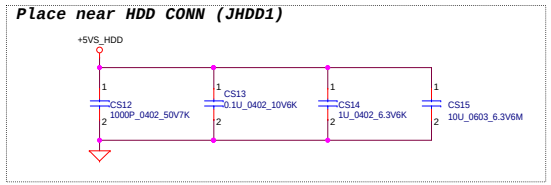
Date: Thursday, August 18, 2016 | Sheet 43 of 70

M.2 Slot-C Key-M (SSD)



HDD CONN





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: SSD

Size: C | Document Number: LA-D991P | Rev: 0.1(000)

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For Dell review only

USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

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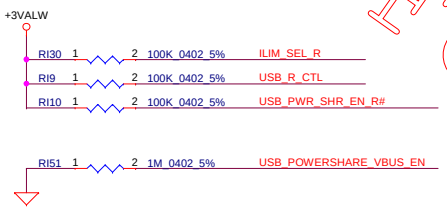
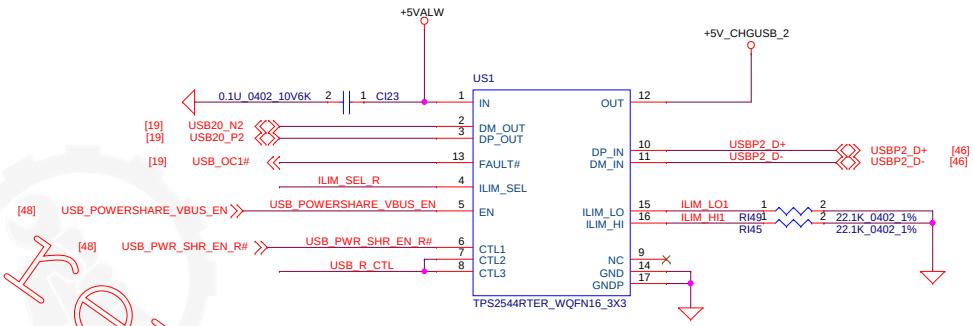
For Dell review only

USB3.0 / USB2.0 Port1





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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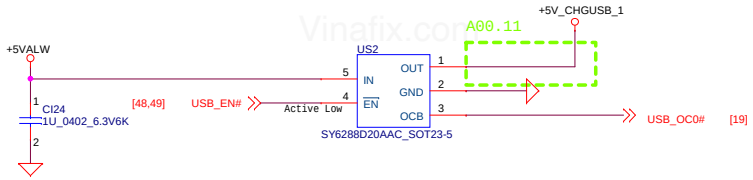
Compal Electronics, Inc.

Title: USB Powershare

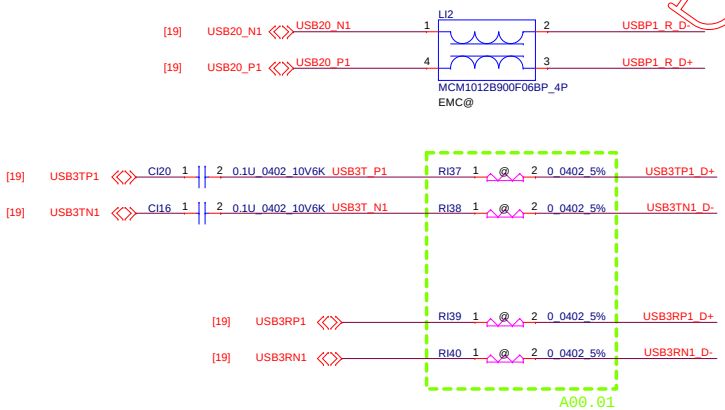
Document Number: LA-D991P

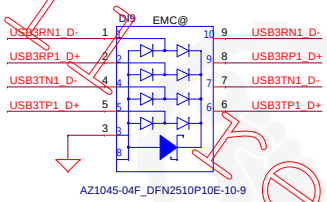
Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 45 of 70

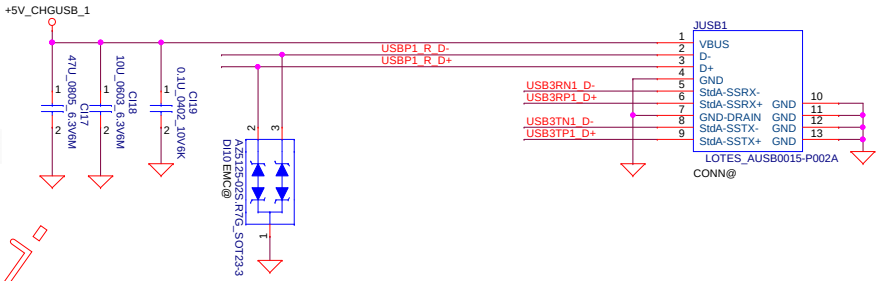


USB3.0 / USB2.0 Port1

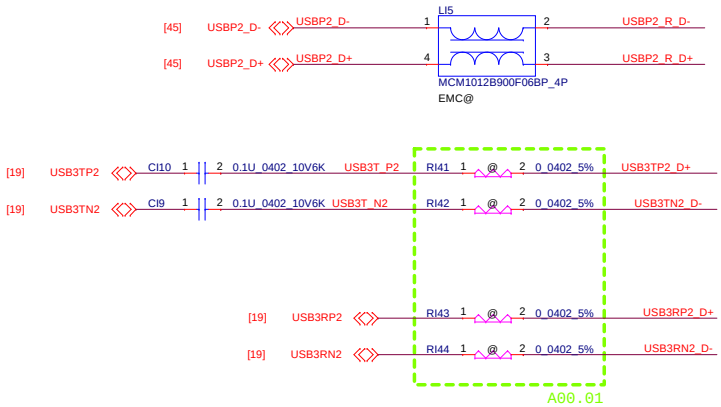


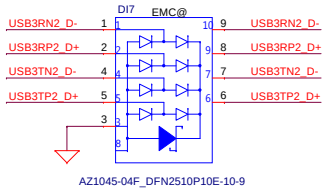


Place close to JUSB1

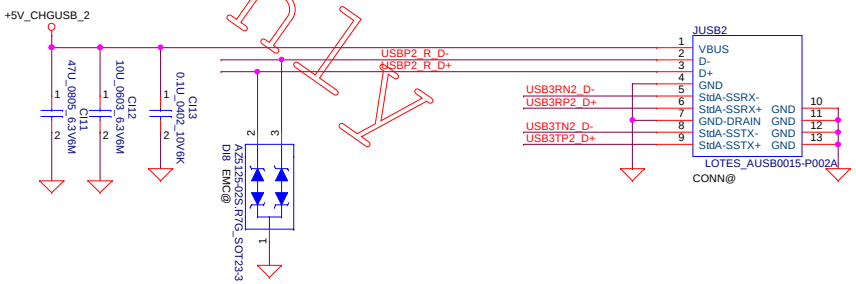


USB3.0 / USB2.0 Port2 (Power share)





Place close to JUSB2



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Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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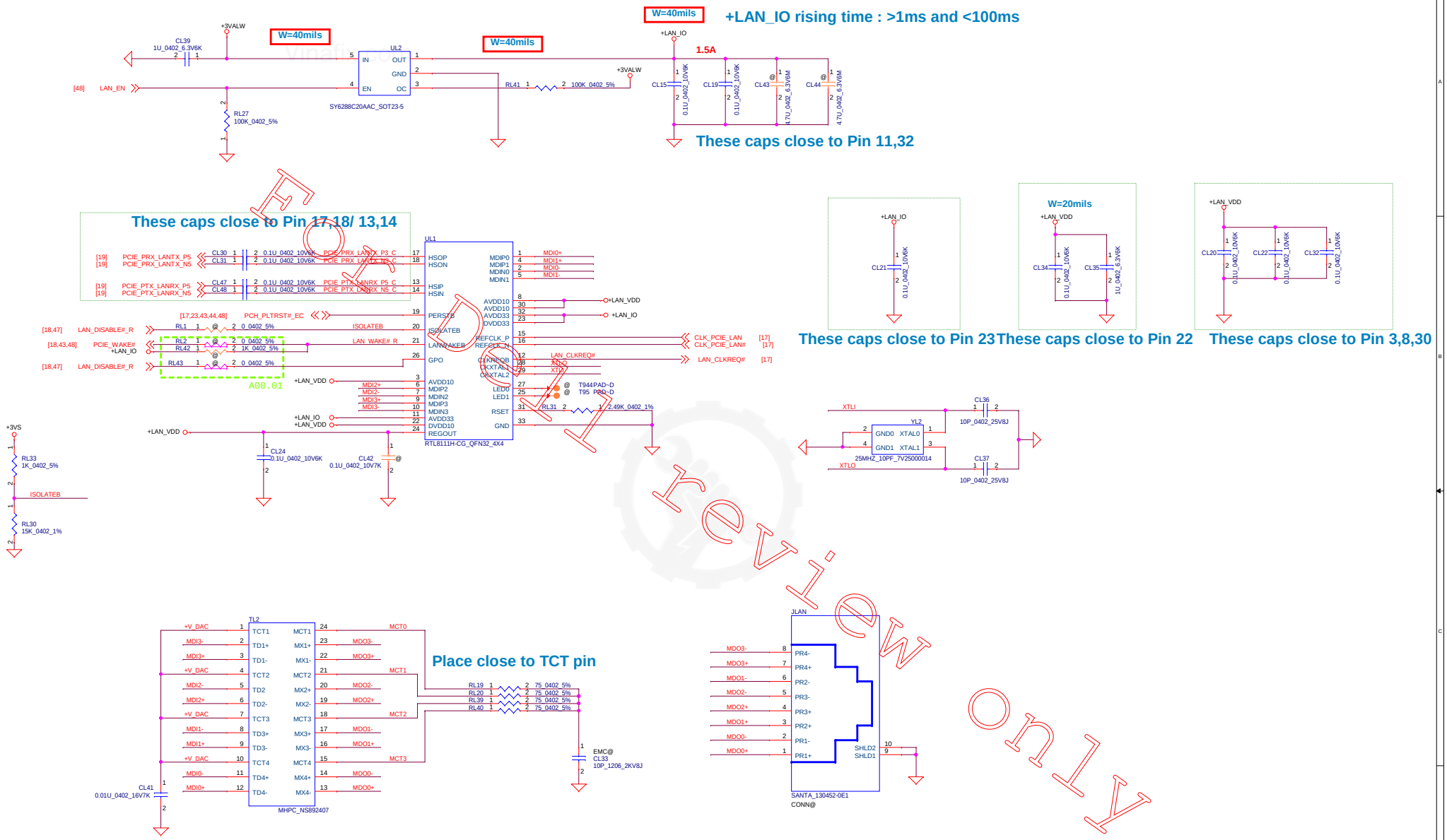
Compal Electronics, Inc.

Title: **USB conn.**

Document Number: **LA-D991P**

Rev: 0.1(0.00)

Date: Thursday, August 18, 2016 | Sheet 46 of 70



Review Only

Security Classification	Compal Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/07/31

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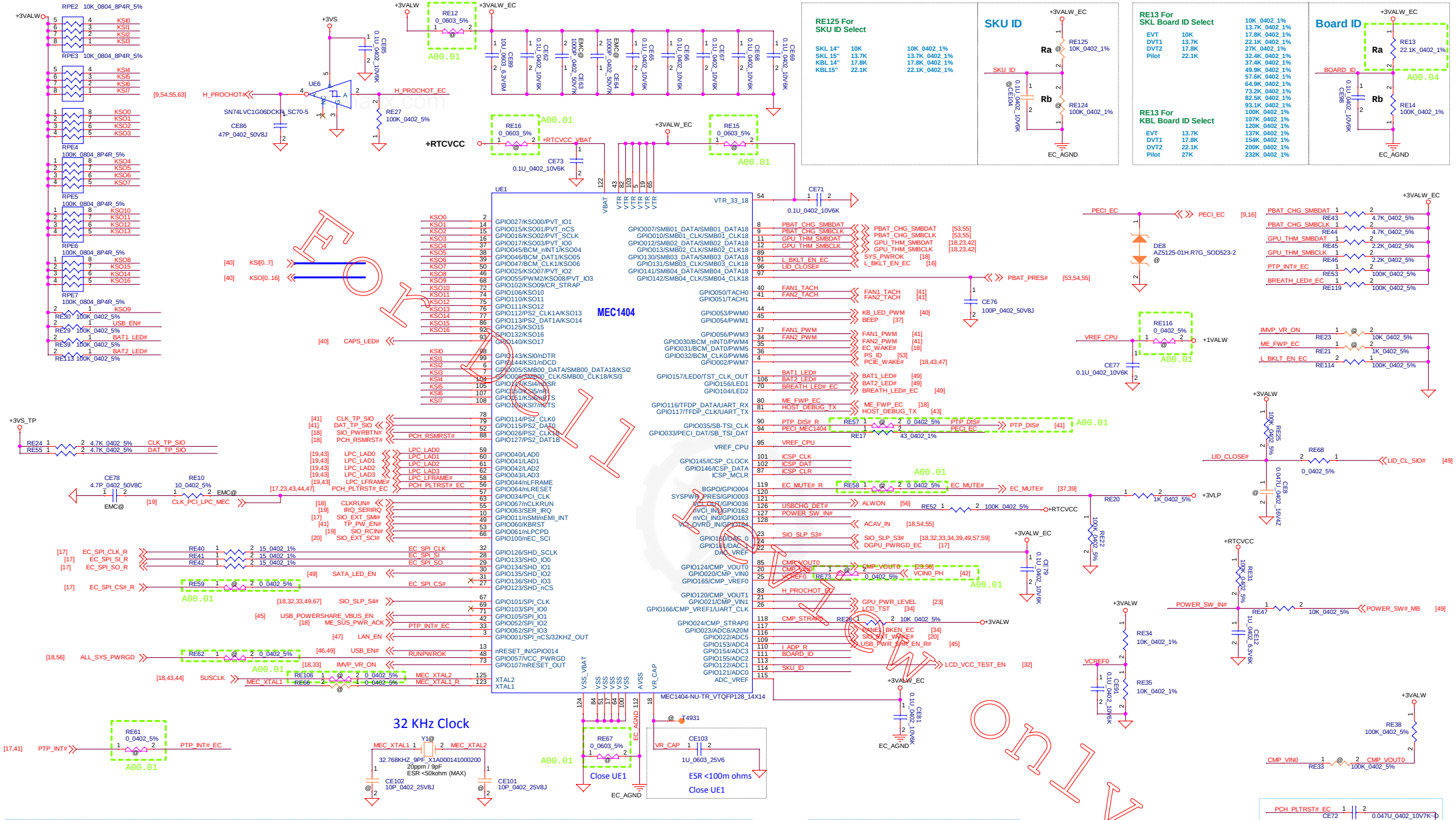
Compal Electronics, Inc.

Title: **LAN RTL8111GUS-CG**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 47 of 70



Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

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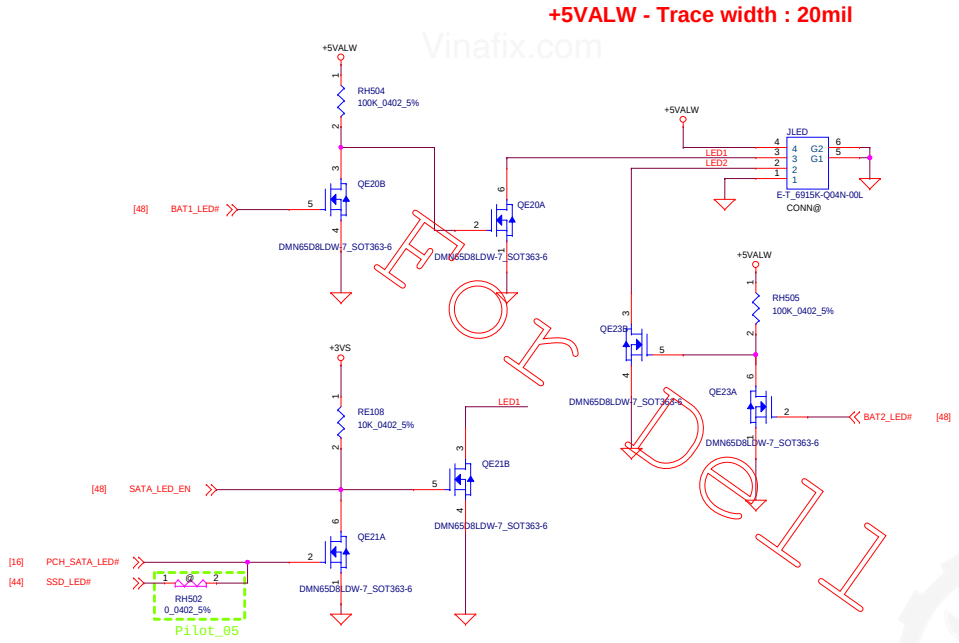
Compal Electronics, Inc.

Title: **EC MEC1404**

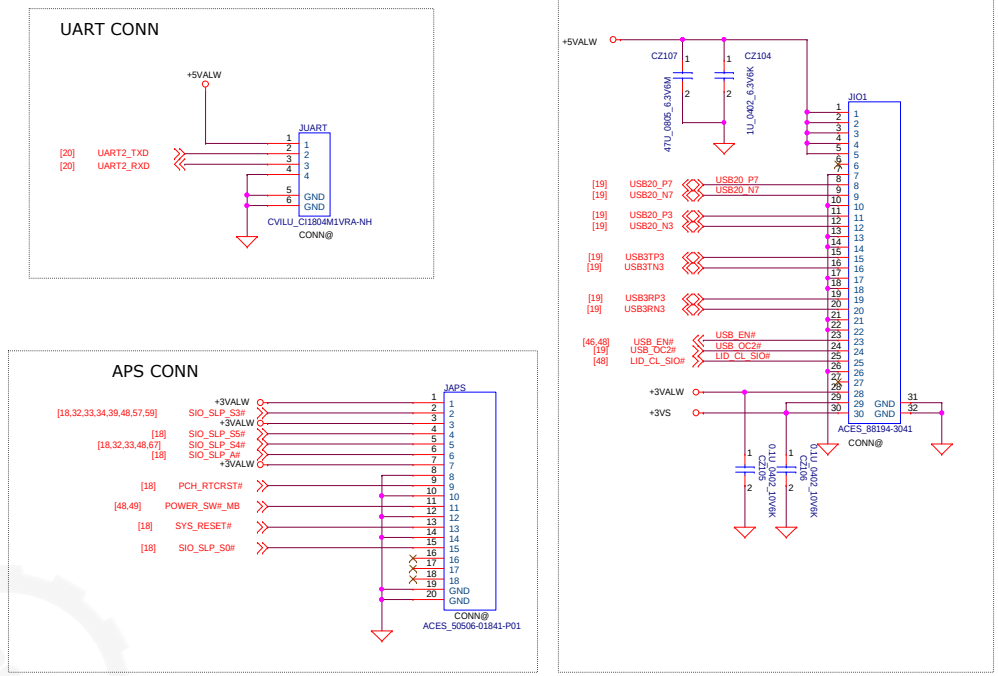
Size: | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 48 of 70

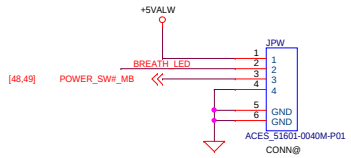
LED Board Connector



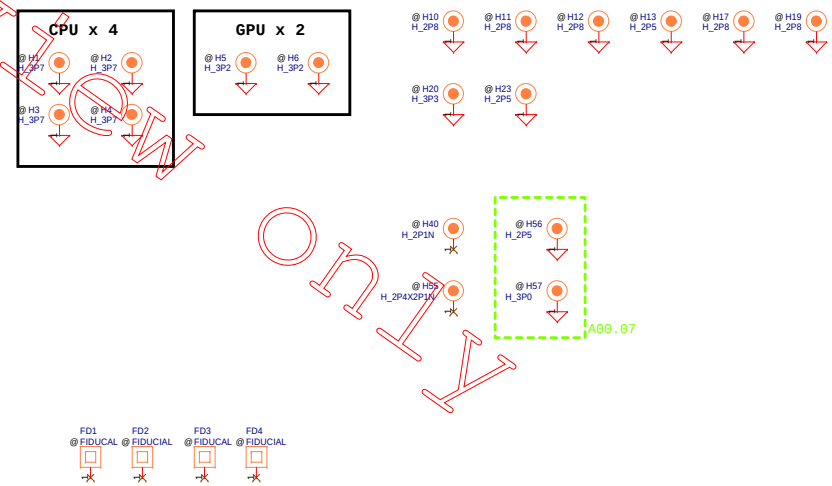
I/O & APS & UART CONN



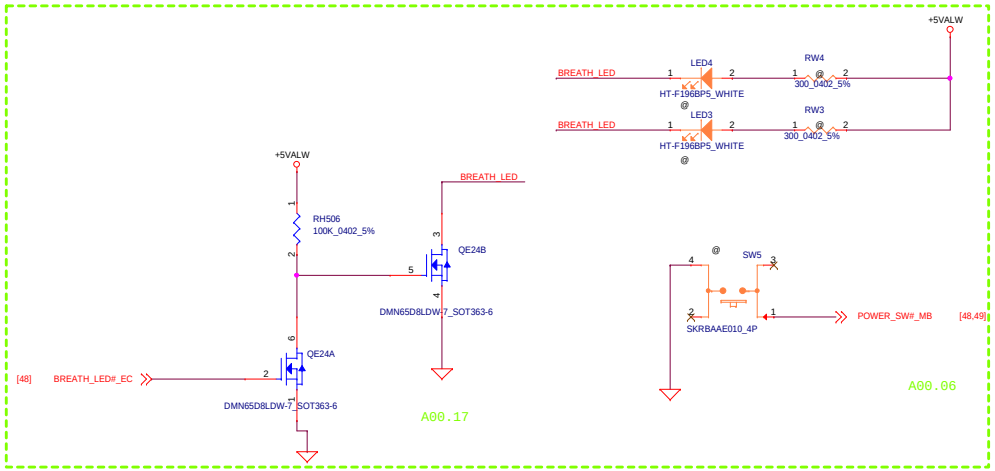
TO PWR BOARD



Screw Hole



Power Button & LED (Reserve)



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Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: **TPM/BTB conn.**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Tuesday, November 01, 2016 | Sheet 49 of 70

MODEL NAME : *BCV00/ BCV10*

PCB NO : *LA-D991P*

Bom Structure

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PCB

ZZZ R1@

PCB 1QT LA-D991P REV0 M/B

CPU

UH1 CPUI5@

SKL-H_SR2FP

UH1 CPUI7@

SKL-H_SR2FQ

UH1 QSCPU@

SKL-H_QJMK

PCH

UH2 R1@

PCH-HM170

GPU

UV1 14GT@

N16P-GT-A2

UV1 15GX@

N16P-GX-A2

Micron 2G *X7668431L02 : M2G@*

RV160 M2G@

24.9K_0402_1%
SD034249280

UV6 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV7 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV8 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV9 EDW4032BABG-70-F-R_FBGA170P~D M2G@

Hynix 2G *X7668431L01 : H2G@*

RV160 H2G@

34.8K_0402_1%
SD034348280

UV6 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV7 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV8 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV9 H5GC4H24AJR-R0C_FBGA170P~D H2G@

Samsung 4G *X7668431L03 : S4G@*

RV157 S4G@

4.99K_0402_1%
SD034499180

UV6 K4G80325FB-HC28_FBGA170P~D S4G@

UV7 K4G80325FB-HC28_FBGA170P~D S4G@

UV8 K4G80325FB-HC28_FBGA170P~D S4G@

UV9 K4G80325FB-HC28_FBGA170P~D S4G@

Micron 4G *X7668431L04 : M4G@*

RV157 M4G@

10K_0402_1%
SD034100280

UV6 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV7 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV8 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV9 MT51J256M32HF-70:A_FBGA170P~D M4G@

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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: *NOTE*

Size | Document Number: *LA-D991P* | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 50 of 70

Version Change List (P. I. R. List) Page 2

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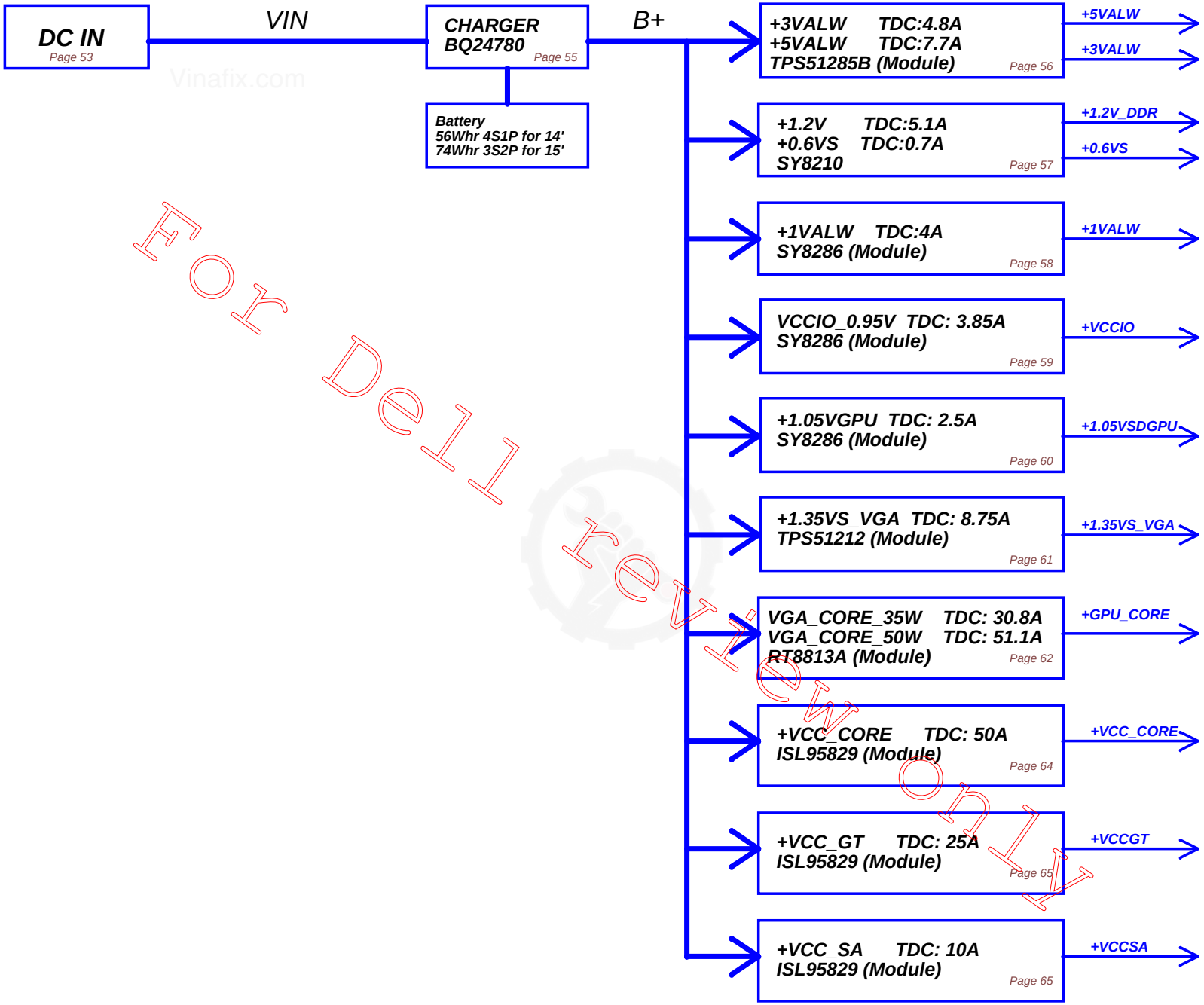
Compal Electronics, Inc.

Title: **NOTE**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 51 of 70



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Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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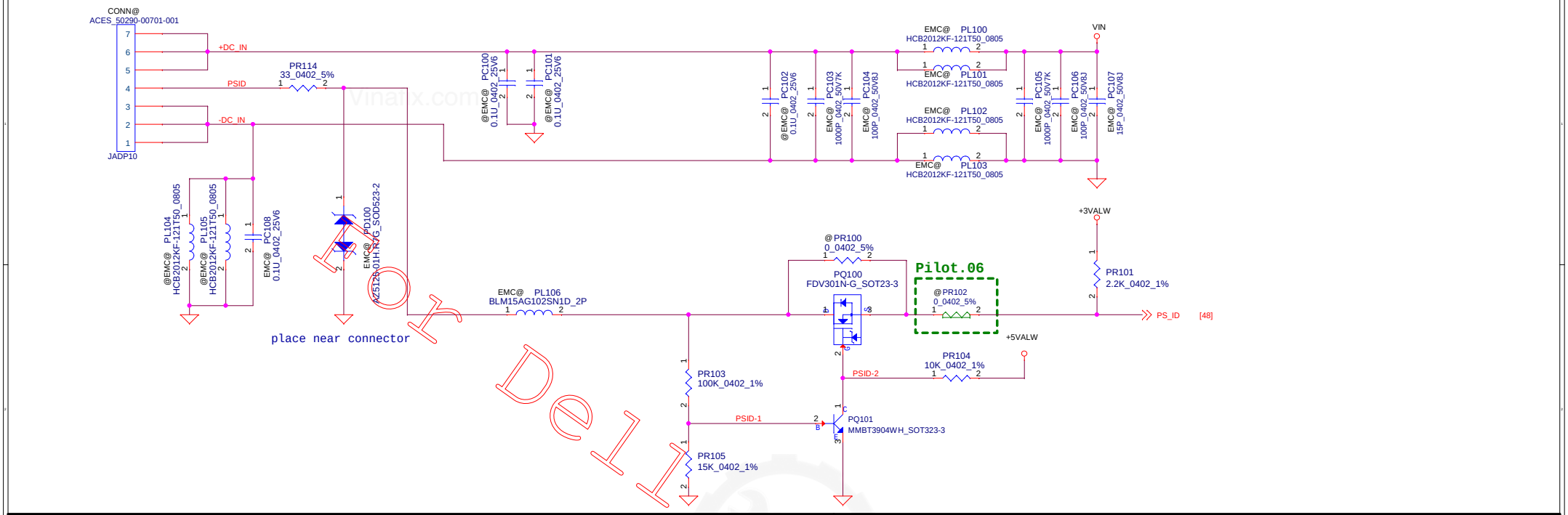
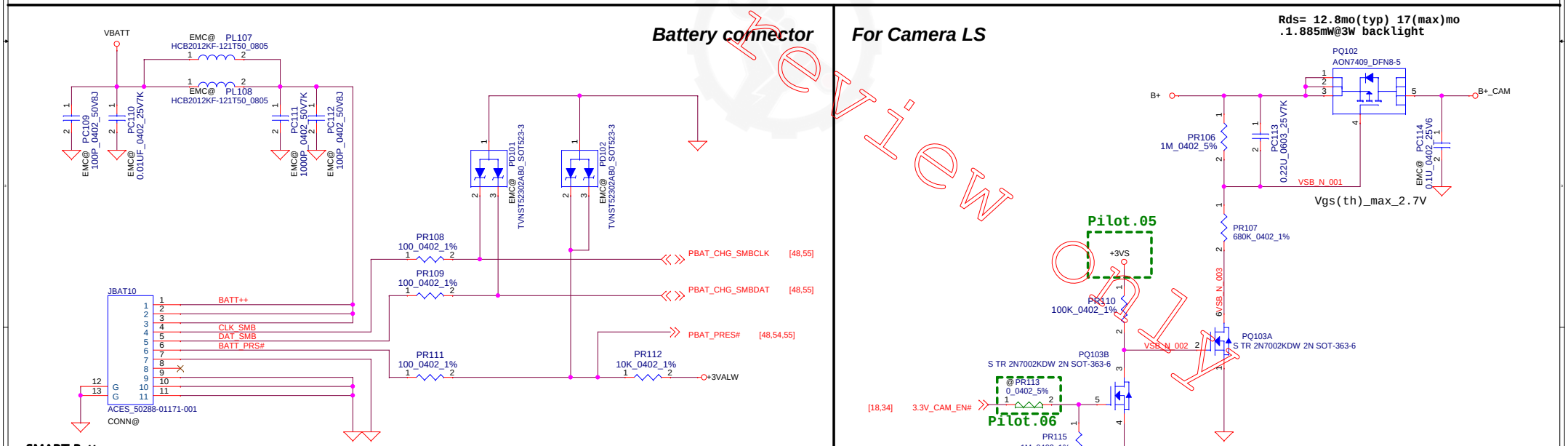
Compal Electronics, Inc.

Title: **Power Block Diagram**

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 52 of 70





SMART Battery:
01.BAT1+
02.BAT2+
03.BAT3+
04.CLK_SMB
05.DAT_SMB
06.BATT_PRS
07.SYS_PRS
08.Battery Voltage
09.GND1
10.GND2
11.GND3

Battery
56Whr 4S1P for 14'
74Whr 3S2P for 15'

Smart Adapter circuit (39.1)

Delivery review only

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

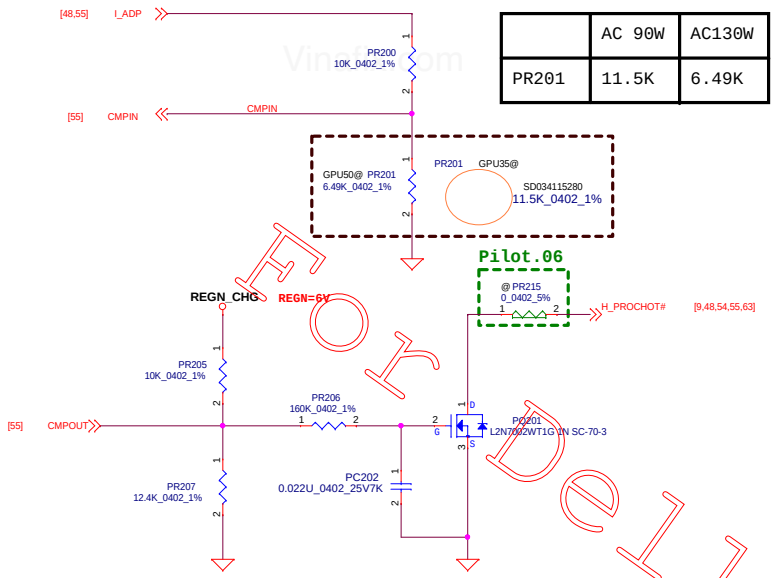
Title: **PWR_DCIN / BATT CONN**

Size | Document Number | Rev 0.1(X00)

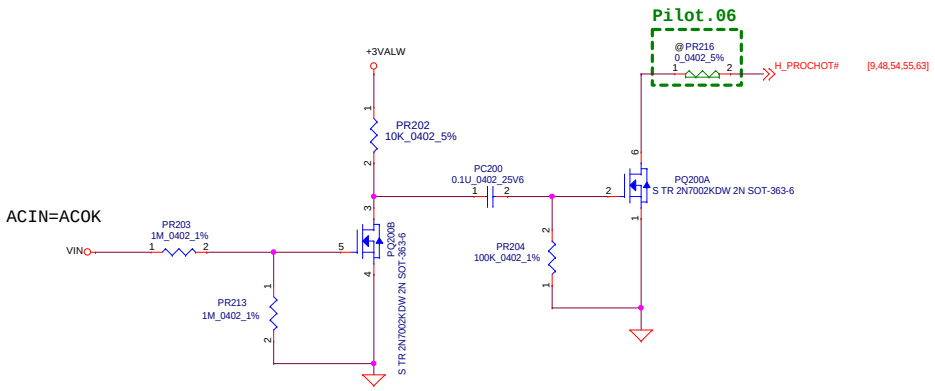
Date: Thursday, August 18, 2016 | Sheet 53 of 70

When CMPIN> Vref(2.3V/1.3V)
CMPOUT=floating

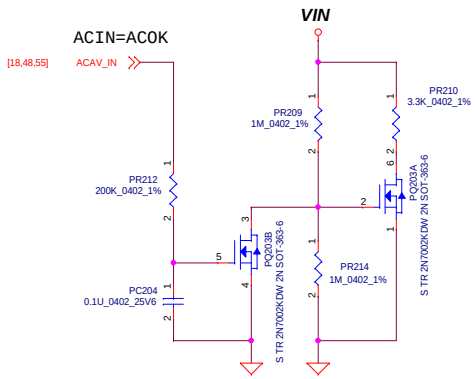
	AC 90W	AC130W
PR201	11.5K	6.49K



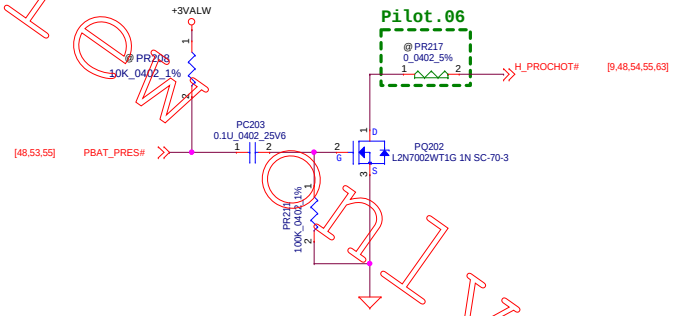
ENG0012879 Circuit-1
Delay Adapter OC H_PROCHOT# 2ms while Hybrid power transition



Ref ENG0012879 Circuit-2
HW Asserts H_PROCHOT# when ac adapter is being unplugged and keep low for 10ms until SW prochot# is issuded by EC



Erp lot 6 circuit



Ref ENG0012879 Circuit-4
HW Asserts H_PROCHOT# when battery is being unplugged and keep low for 10ms until SW prochot# is issuded by EC

Rest of support elements (37.1)

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Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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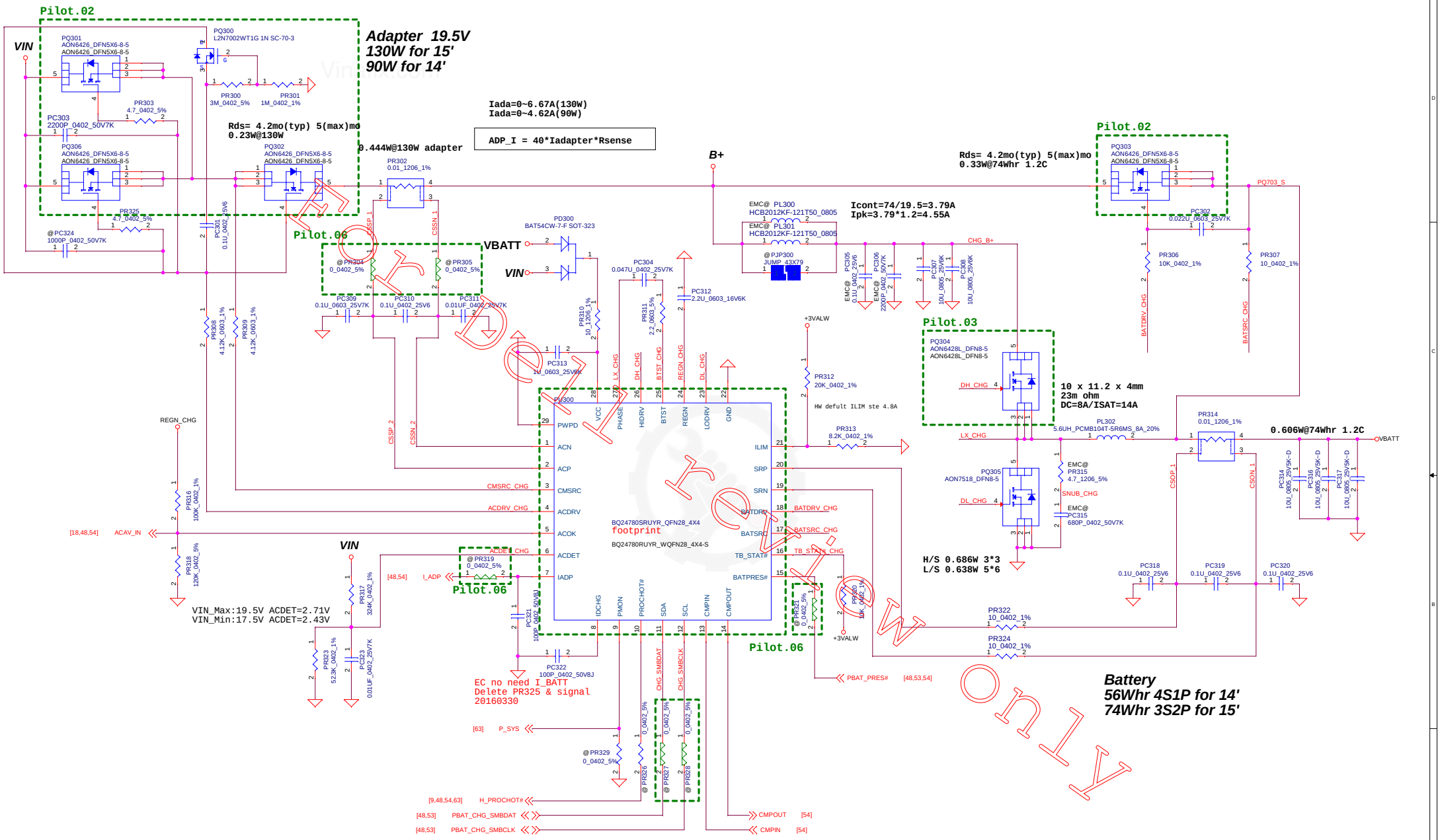
Title: PWR_PROCHOT#

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 54 of 70



Security Classification	Compal Secret Data		
Issued Date	2013/11/05	Deciphered Date	2015/11/05

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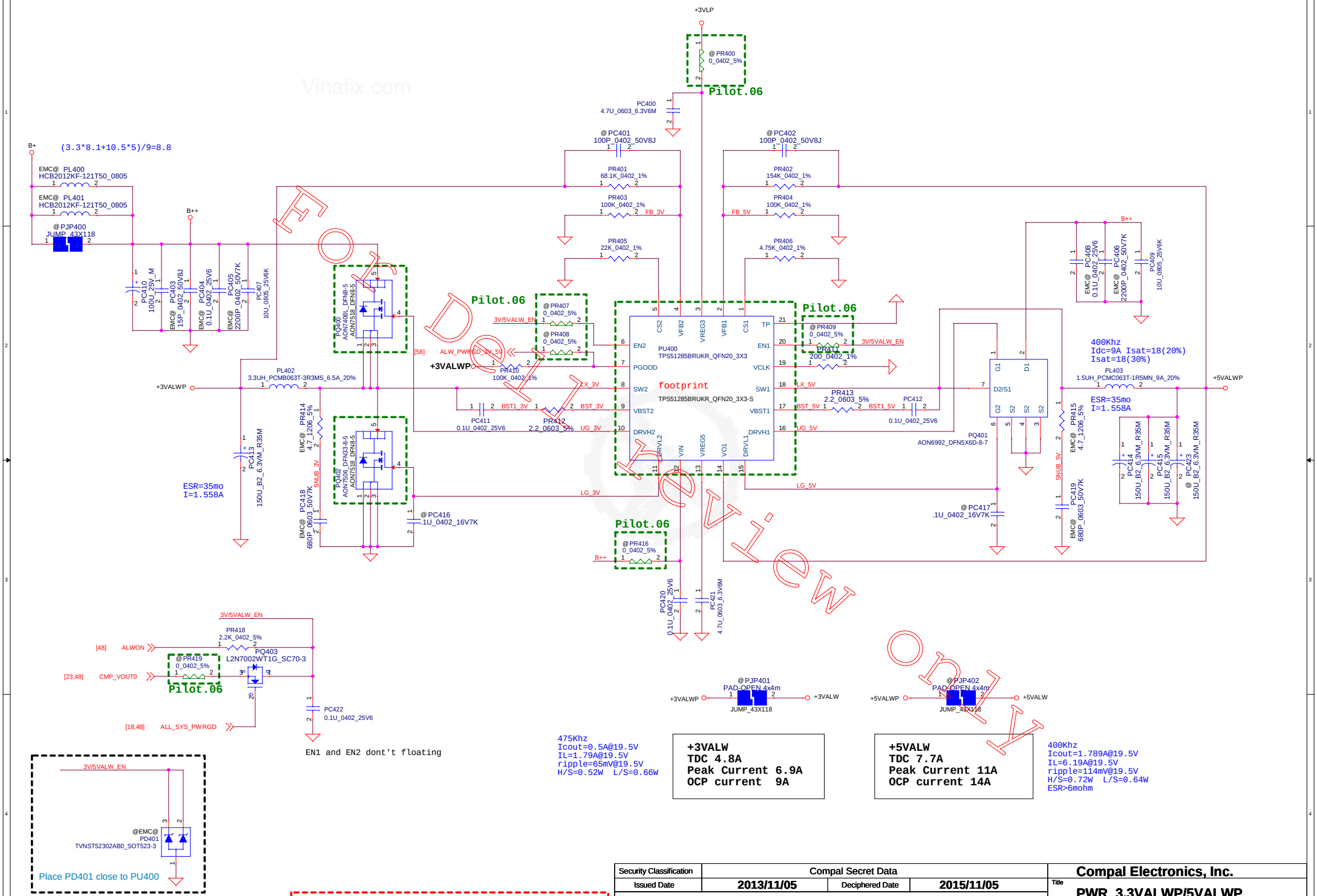
Compal Electronics, Inc.

Title: **PWR_CHARGER(BQ24780S)**

Size: Custom | Document Number | Rev: 0.1(100)

Date: Thursday, August 18, 2016 | Sheet 55 of 70



Security Classification	Compal Secret Data		
Issued Date	2013/11/05	Deciphered Date	2015/11/05

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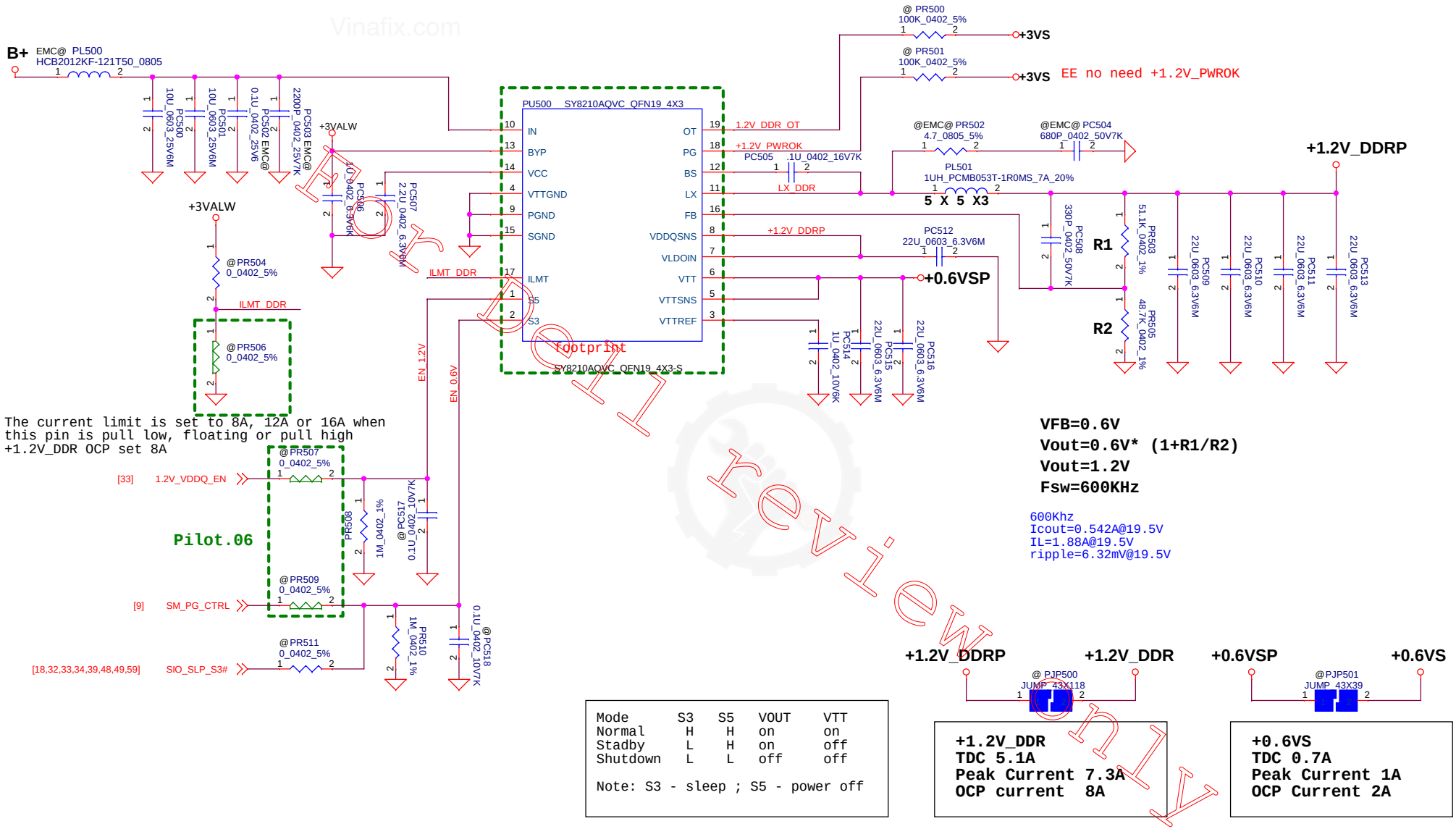
Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

Size: Custom | Document Number | Rev: 0.1(100)

Date: Thursday, August 18, 2016 | Sheet 56 of 70



Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

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Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

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Compal Electronics, Inc.

Title: **PWR_+1.2V_DDR/0.6VS(SY8210)**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 57 of 70

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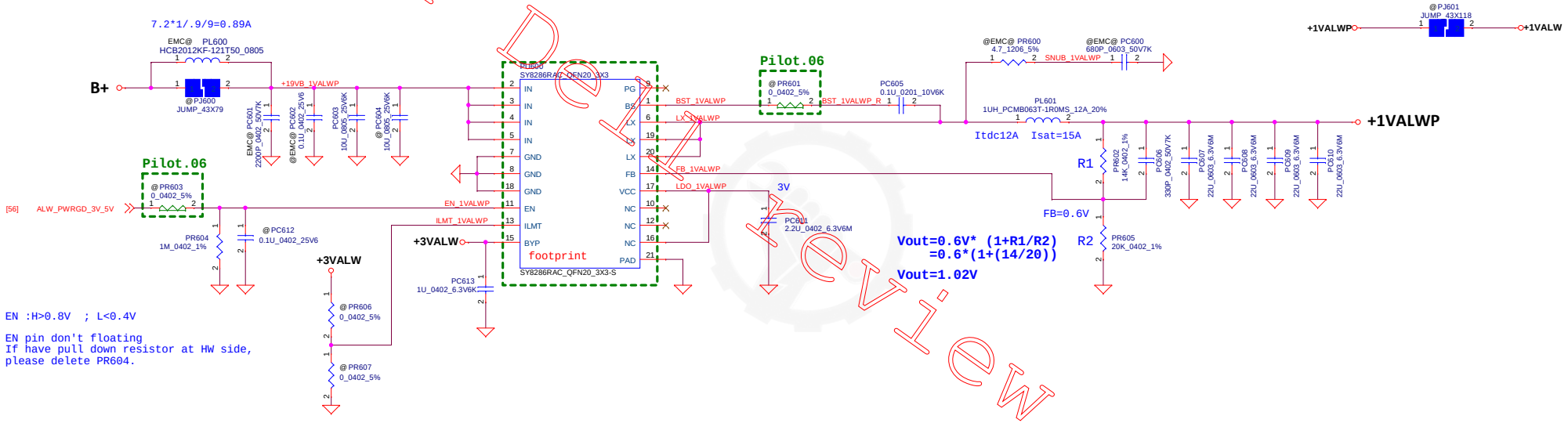
+1VALW
TDC 4A
Peak Current 5.7A
OCP current 9A

500Khz
IL=1.9A@19.5V
ripple=7.3mV@19.5V

7.2*1/.9/9=0.89A



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR604.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

PWR.Plane.Regulator(35.25), Support component(35.26)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **PWR_+1VALW (SY8288)**

Size: | Document Number: **LA-D991P** | Rev: 0.1(00)

Date: Thursday, August 18, 2016 | Sheet 58 of 70

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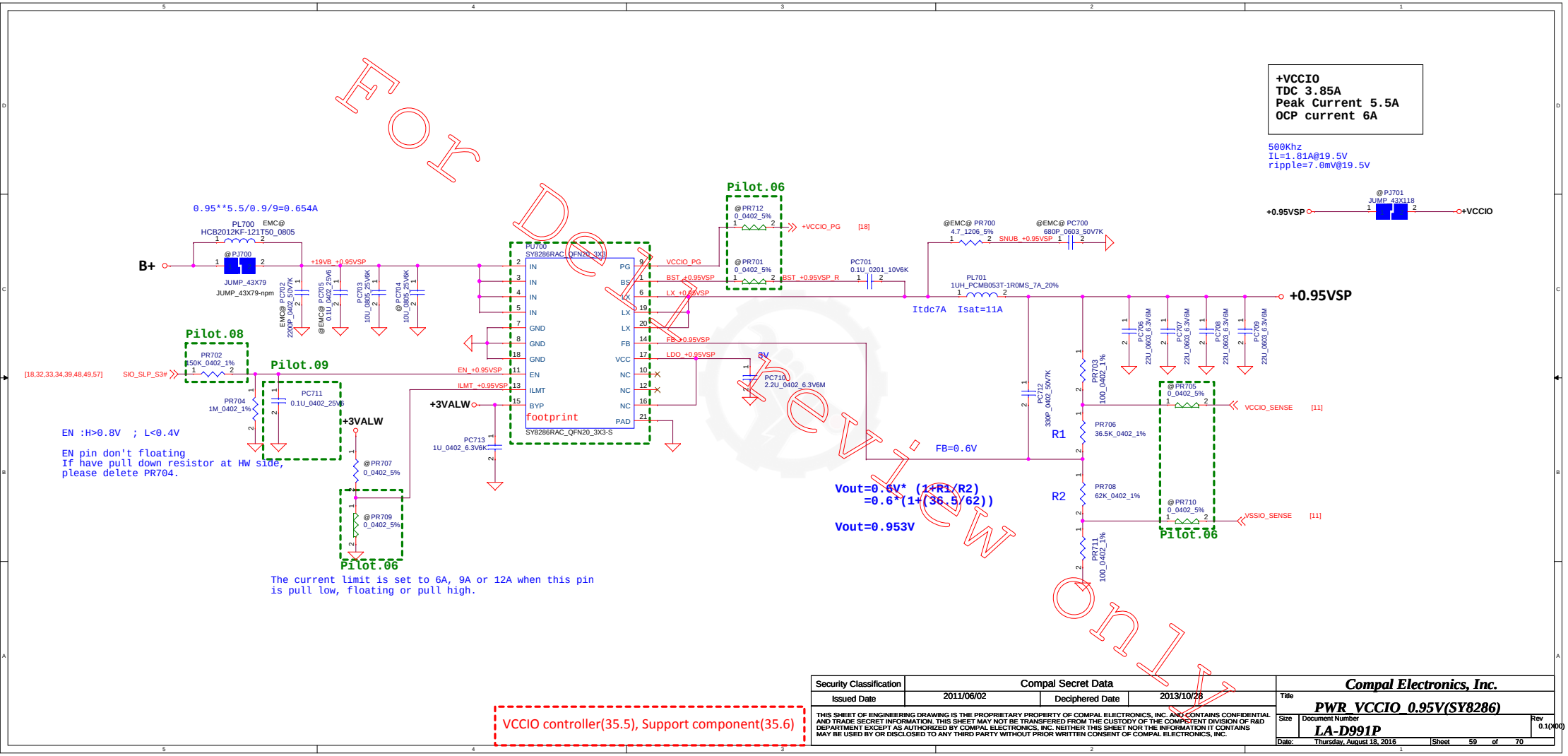

VCCIO controller(35.5), Support component(35.6)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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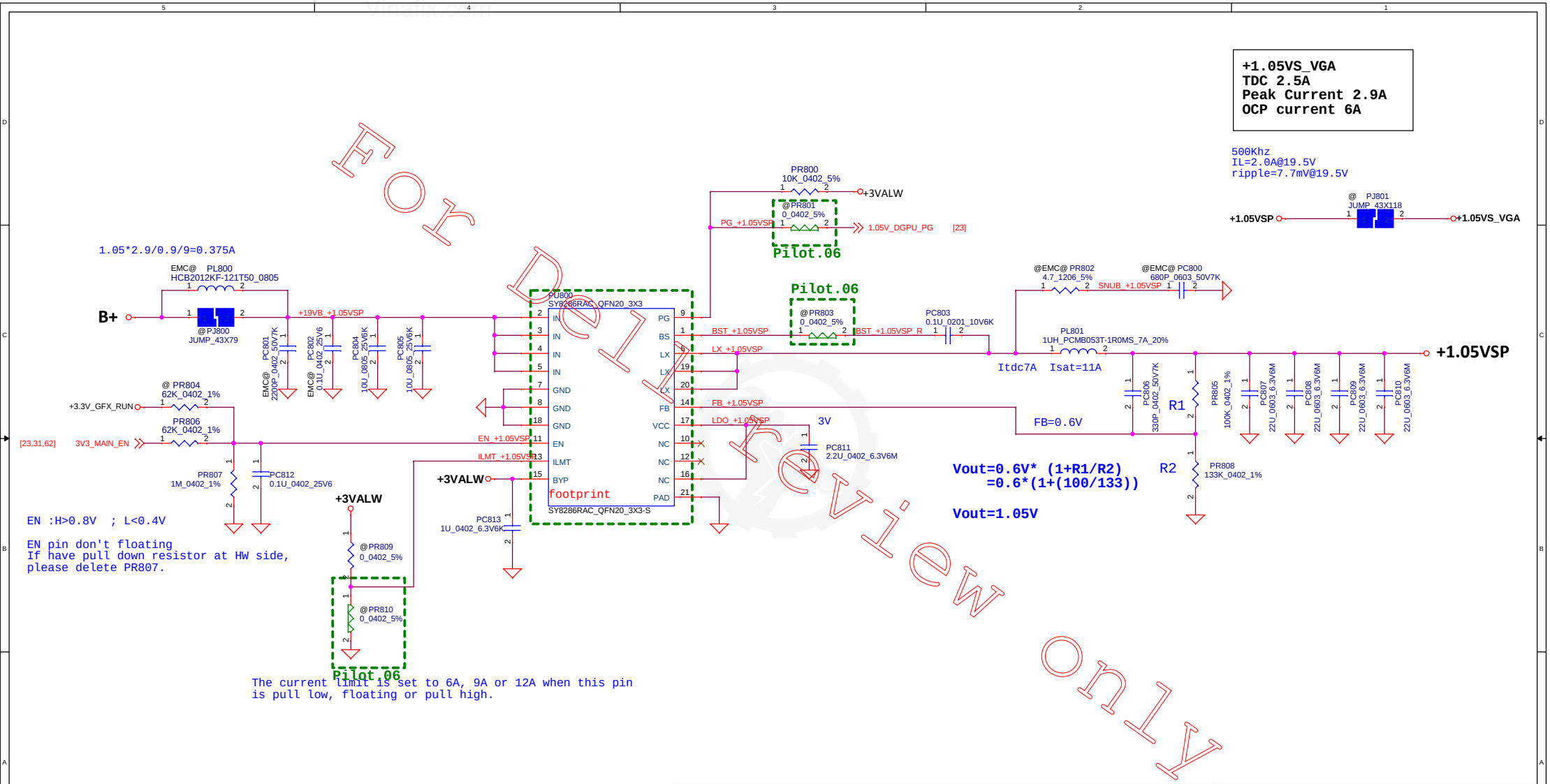
Compal Electronics, Inc.

Title: PWR_VCCIO_0.95V(SY8286)

Size: LA-D991P | Document Number | Rev 0.1(00)

Date: Thursday, August 18, 2016 | Sheet 59 of 70



GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **PWR_+1.05VGPU(SY8286)**

Size: | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 60 of 70

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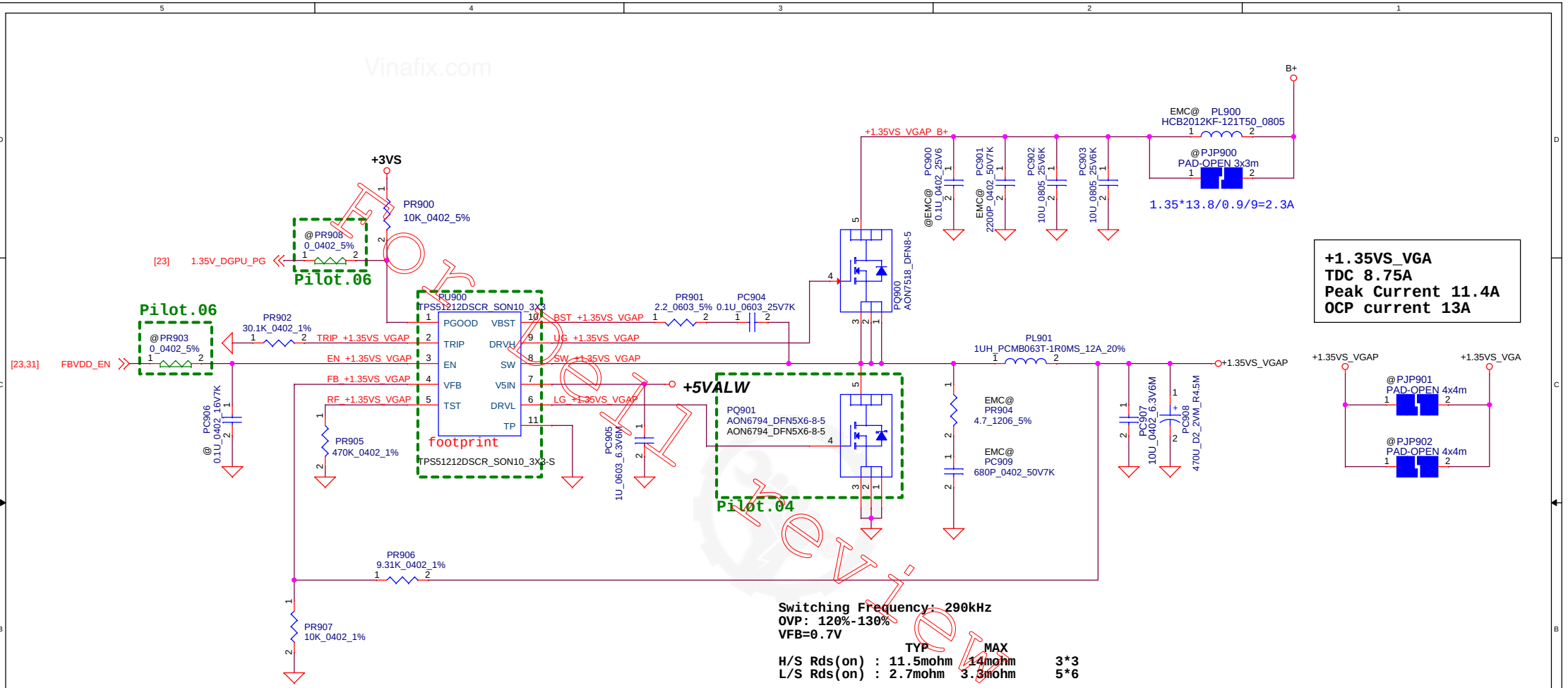

GPU other power_Regulatorr(43.5), Support component(43.6)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **PWR_+1.35VDGPU(TPS51212)**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 61 of 70

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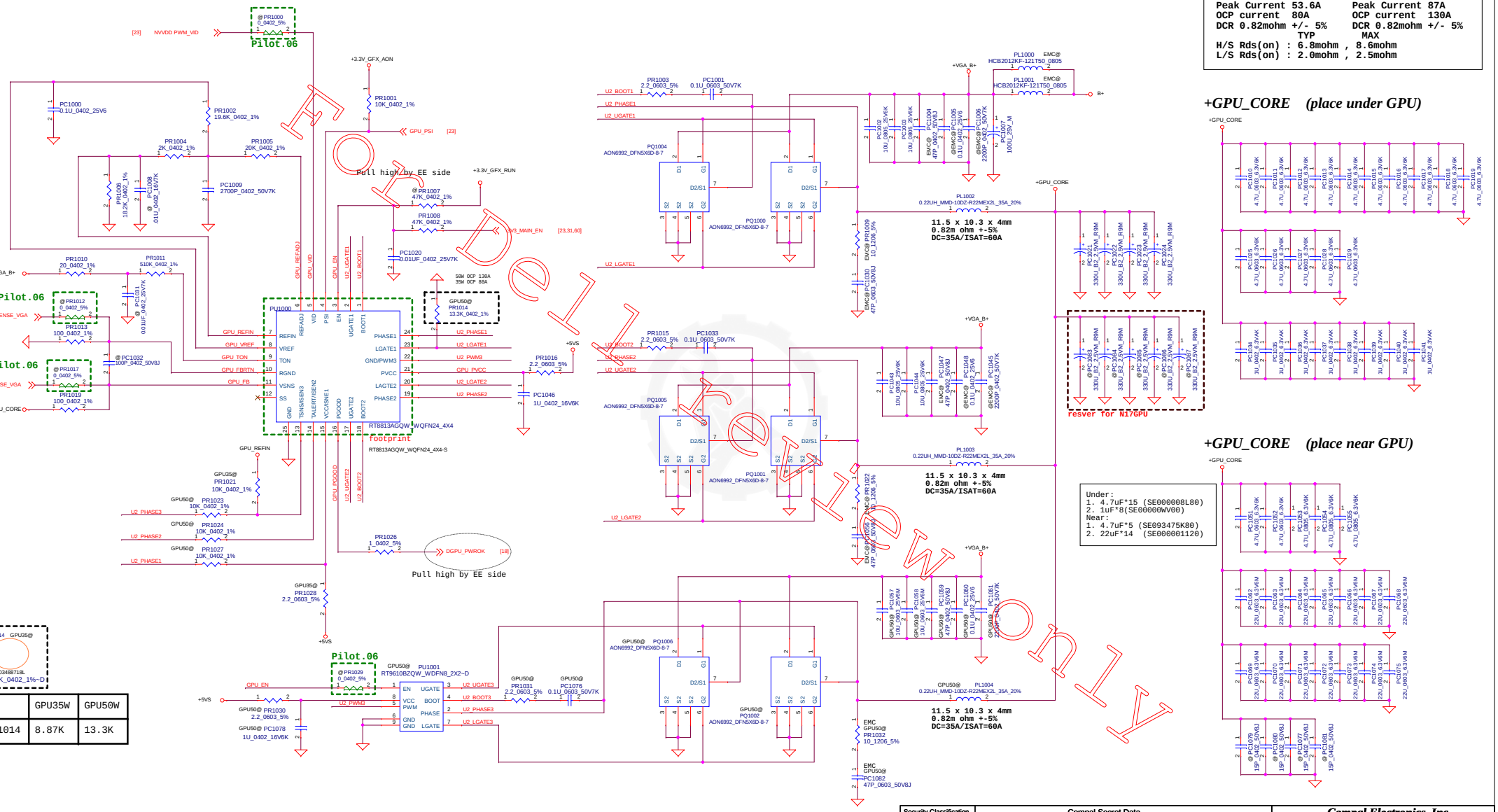
GPU_CORE (0.95V)	GPU_CORE (0.95V)
N16P-GT GDDR5_30W	N16P-GX GDDR5_50W
TDC 30.8A	TDC 51.1A
Peak Current 53.6A	Peak Current 87A
OCP current 80A	OCP current 130A
DCR 0.82mohm +/- 5%	DCR 0.82mohm +/- 5%
TYP	MAX
H/S Rds(on) : 6.8mohm ,	8.6mohm
L/S Rds(on) : 2.0mohm ,	2.5mohm



	GPU35W	GPU50W
PR1014	8.87K	13.3K

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Title: PWR_+1.35VDGPU(TPS51212)

Size: A3 | Document Number: LA-D991P | Rev: 0.1(00)

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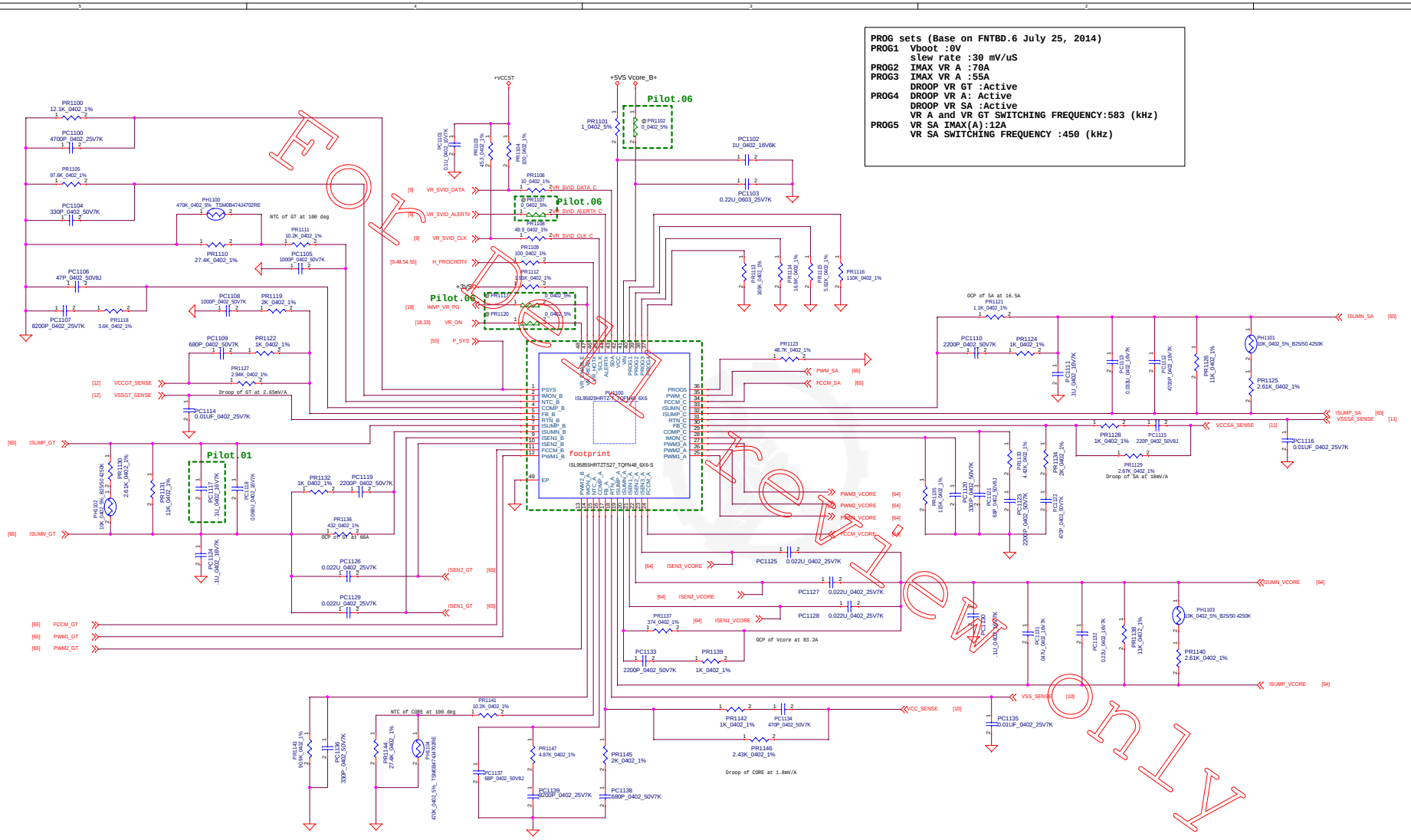

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **PWR-VCORE_ISL95829**

Size: | Document Number: **LA-D991P** | Rev: 0.1(0)

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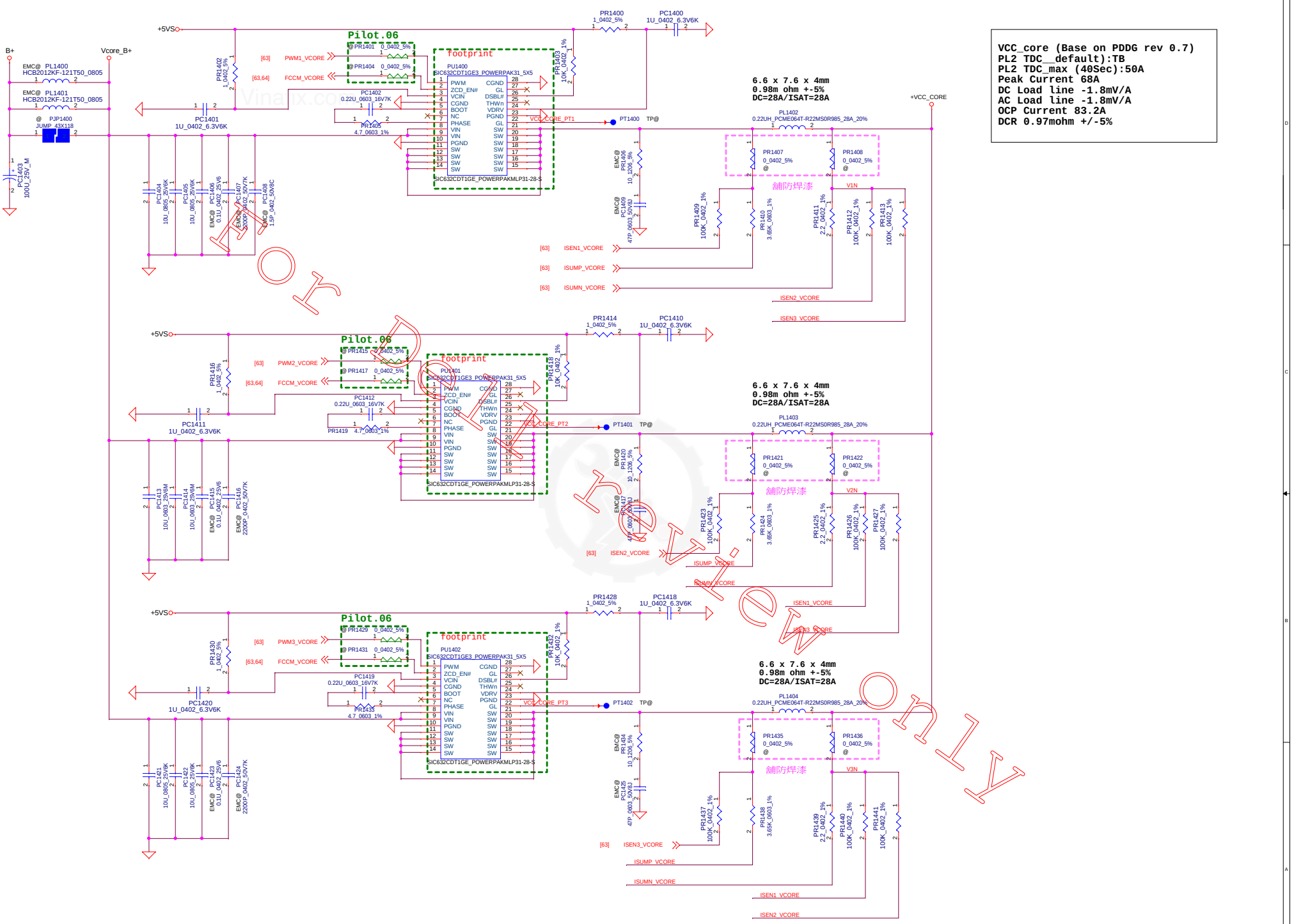

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Title: **PWR-VCORE_VCORE**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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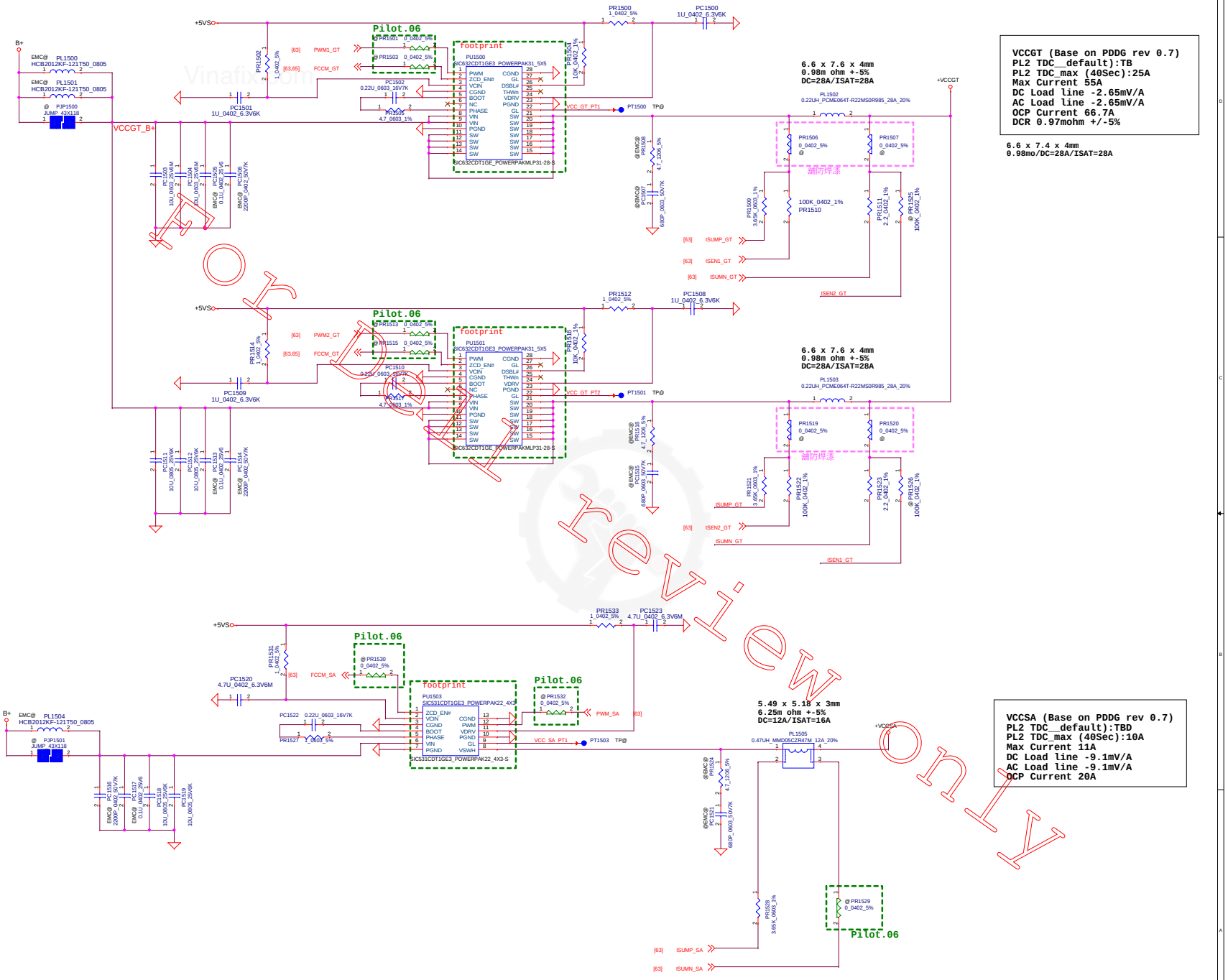

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

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Issued Date	2011/06/02	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **PWR_VCORE_VGT,VSA**

Size: | Document Number: **LA-D991P** | Rev: 0.1(000)

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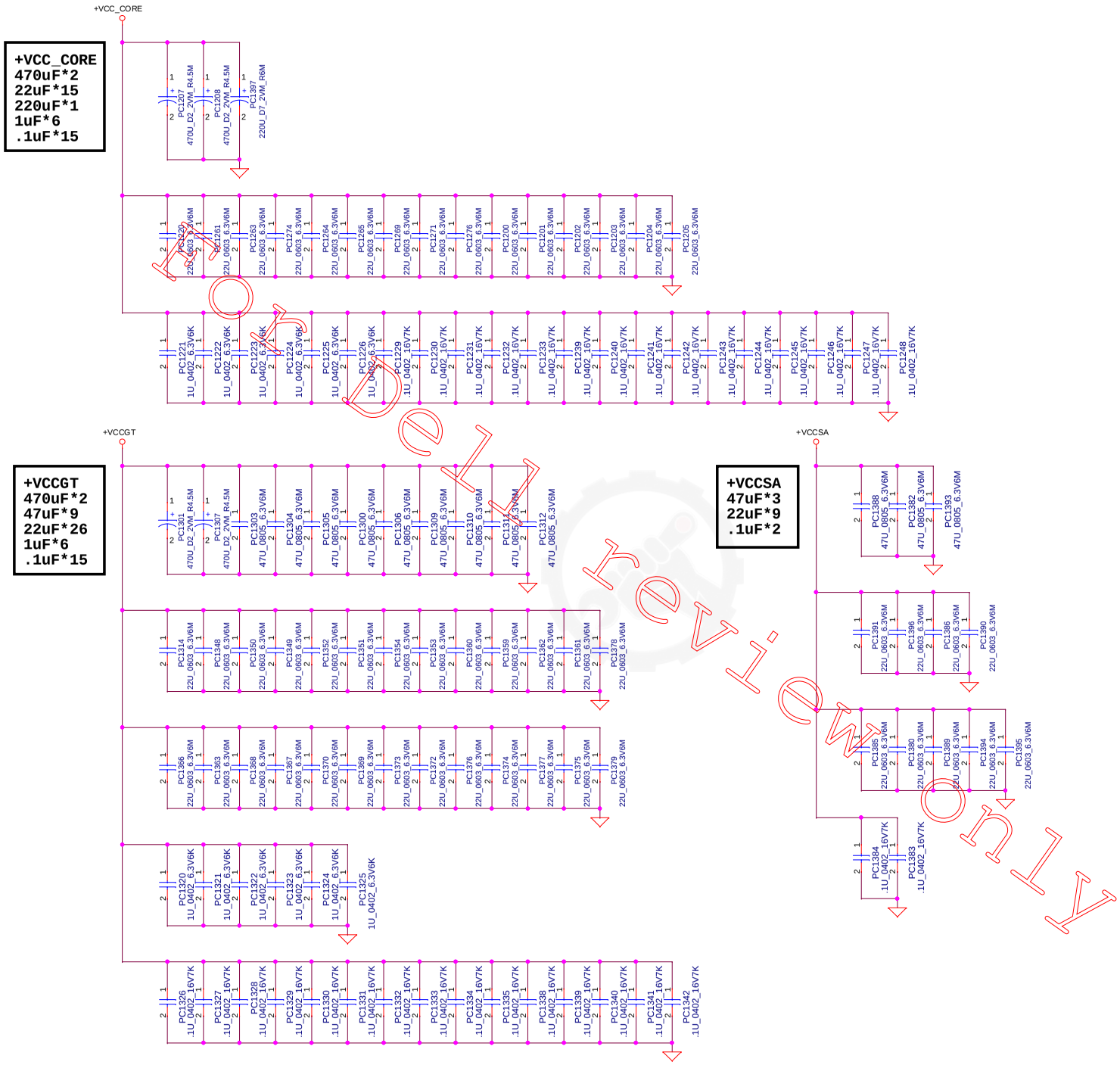

Vcc_CORE output CAP(36.4), Vcc_GT output CAP(36.5), Vcc_SA output CAP(36.6)

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Issued Date	2011/06/02	Deciphered Date	2013/10/28

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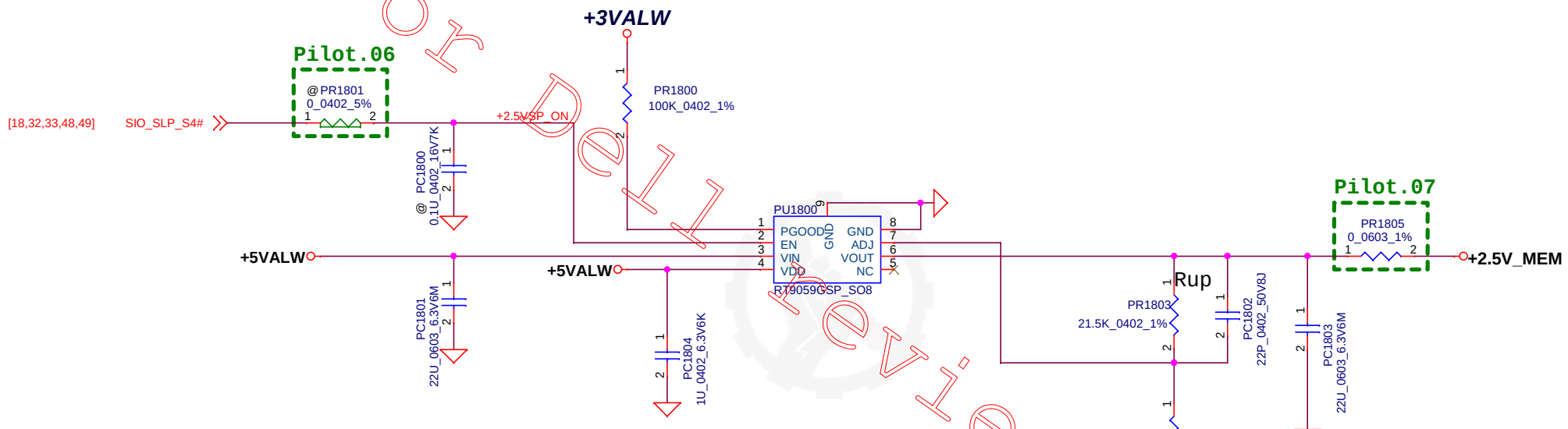
2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A



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Title: **PWR_+2.5V_MEM**

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